

# Compal Confidential

## EH7LW/EH5LW/FH5TW/EH7LC/EH5LC

### DIS MB Schematic Document

### LA-H791P

Rev: 2.0  
2019.05.29

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title Cover Sheet	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number EH7LW M/B LA-H791P
				Date: Thursday, June 06, 2019	Sheet 1 of 57

WWW.ALISALER.COM

HDMI Conn.



page 29

DDI2

HDMI x 4 lanes

eDP



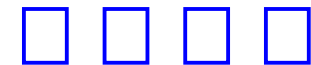
page 28

eDP

DDI

Interleaved Memory

DDR4-ON BOARD 4G 8Gb x16



page 19

260pin DDR4-SO-DIMM X1



page 20

Memory BUS

Dual Channel

1.2V DDR4 2400

Nvidia N17S-G0/G2  
with GDDR5 x2

page 21~27

PCIe 3.0 x 4  
8GT/s  
port 1-4SATA Gen 3  
6.0 Gb/s  
(SATA2)PCIe 3.0 x4  
8GT/s  
Port 9-12

page 31

Flexible IO

Base-U PCIe 3.0x2 (CML)

PCIe 1.0  
2.5GT/s  
port 6

page 31

PCIe 1.0  
2.5GT/s  
port 5LAN(GbE)  
Realtek 8111H

page 30

RJ45 conn.

SATA HDD  
Conn.

page 33

SATA ODD  
Conn.Intel Whiskey lake U  
Intel Comet lake U

Processor

Cannon Lake PCH-LP

46x24 mm

15W

1528pin BGA

page 07~18

WHL-U 4+2  
WHL-U 2+2

LPC/eSPI BUS

CLK=24MHz

ENE  
KB9022

page 36

Int.KBD



page 37

Touch Pad

PS2 (from EC) / I2C (from SOC)  
USB2 port 8 (FP)

page 37

USB 3.0  
conn x1  
USB3 port 1  
USB2 port 1

page 35

USB 2.0  
conn x2  
USB2 port2 (MB)  
USB2 port4(SUB)

page 35

CMOS  
Camera  
USB2 port 7

page 28

Card Reader  
RTS5140  
Reserved

USB2 port 6(SUB)

Finger  
Printer  
USB2 port 5

USB2 port 5

USBx8 48MHz

HD Audio

3.3V 24MHz

HDA Codec  
ALC255

page 32

Touch  
Screen

USB2 port 3

page 28

Int. Speaker

page 32

Int. DMIC  
on Camera

page 28

UAI

page 35

Sub Board

LS-H802P  
HDD/B

page 33

LS-H783P  
LID/B

page 38

LS-H781P  
IO/B

page 38

LS-H784P  
ODD/B

page 33

Fan Control

page 39

RTC CKT.

page 15

Power On/Off CKT.

page 37

DC/DC Interface CKT.

page 40

Power Circuit DC/DC

page 41~54

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Block Diagrams	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number
				Date: Thursday, June 06, 2019	EH7LW M/B LA-H791P
				Sheet 2 of 57	0.2

WWW.ALISALER.COM

<b>Vcc</b>	<b>3.3V +/- 5%</b>					
<b>Ra</b>	<b>100K +/- 1%</b>					
<b>Board ID</b>	<b>Rb</b>	<b>V<sub>BID</sub> min</b>	<b>V<sub>BID</sub> typ</b>	<b>V<sub>BID</sub> max</b>	<b>EC AD3</b>	<b>PCB Revision</b>
<b>0</b>	<b>0</b>	<b>0 V</b>	<b>0 V</b>	<b>0.300 V</b>	<b>0x00 - 0x13</b>	<b>0.1(EVT)</b>
<b>1</b>	<b>12K +/- 1%</b>	<b>0.347 V</b>	<b>0.345 V</b>	<b>0.360 V</b>	<b>0x14 - 0x1E</b>	<b>0.2(DVT)</b>
<b>2</b>	<b>15K +/- 1%</b>	<b>0.423 V</b>	<b>0.430 V</b>	<b>0.438 V</b>	<b>0x1F - 0x25</b>	<b>0.3(PVT)</b>
<b>3</b>	<b>20K +/- 1%</b>	<b>0.541 V</b>	<b>0.550 V</b>	<b>0.559 V</b>	<b>0x26 - 0x30</b>	<b>1.0(PreMP)</b>
<b>4</b>	<b>27K +/- 1%</b>	<b>0.691 V</b>	<b>0.702 V</b>	<b>0.713 V</b>	<b>0x31 - 0x3A</b>	
<b>5</b>	<b>33K +/- 1%</b>	<b>0.807 V</b>	<b>0.819 V</b>	<b>0.831 V</b>	<b>0x3B - 0x45</b>	
<b>6</b>	<b>43K +/- 1%</b>	<b>0.978 V</b>	<b>0.992 V</b>	<b>1.006 V</b>	<b>0x46 - 0x54</b>	
<b>7</b>	<b>56K +/- 1%</b>	<b>1.169 V</b>	<b>1.185 V</b>	<b>1.200 V</b>	<b>0x55 - 0x64</b>	

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CODEC	255@/256@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
CNVi /BT PCM Select	CNVI@/PCM@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
TPM	TPM@
Finger Print	FP@/FPFMC@
Finger print power	FP3V@/FP5V@
UMA or DGPU	UMA@/VGA@
CPU Select	WHL@/CML@
SATA/ODD select	RD@/NRD@/ODD@
USB charger	CHG@

BOM Option Table	
Item	BOM Structure
MB Stage	EVT@/DVT@/PVT@/MP@
G Sensor	GSEN@
For over 3 cell battery	3S@
MD BOM Select	NOX76@/X76DSAM@/ X76DMIC@/X76DHYN@/
VRAM BOM Select	X76VSAM@/X76VMIC@/ X76VHYN@/
Memory related	SPD@/DDP@/MEM@
CPU C10 support	C10@
BOM select	15DIS@/15@/
VGA chip	G0@/G2@

43 Level	Description	BOM Structure
431AHVBOL01	SMT MB AH791 EH7LW I37020U22 230 HDMI	8145U@/PCB@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VHYNe/NC10@/CNV1@/NCHG@/FP@/3S@/LPC@/CMC@/GSENe/RD@/ODD@/255@/BYOC@/TPM@/EVT@/X4@/15@/15DIS@/FP3V@
431AHVBOL02	SMT MB AH791 EH7LW I38130U42 250 HDMI	8265U@/PCB@/MEM@/SDP@/X76DHYNe/VGA@/G2@/X76VHYNe/NC10@/CNV1@/NCHG@/FP@/3S@/LPC@/CMC@/GSENe/RD@/ODD@/255@/BYOC@/TPM@/EVT@/X4@/15@/15DIS@/FP3V@
431AHVBOL03	SMT MB AH791 EH7LW I38145U22 230 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VHYNe/NC10@/CNV1@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4@/15@/15DIS@/FP3V@
431AHVBOL04	SMT MB AH791 EH7LW I58265U42 230 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VHYNe/NC10@/CNV1@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4@/17@/15DIS@/FP3V@
431AHVBOL05	SMT MB AH791 EH7LW I38145U22 230V8 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VSAM@/NC10@/CNV1@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4@/17@/15DIS@/FP3V@
431AHVBOL06	SMT MB AH791 EH7LW I58265U42 230V8 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VSAM@/NC10@/CNV1@/NCHG@/RD@/ODD@/3S@/LPC@/CMC@/255@/DVT@/X4@/17@/15DIS@/FP3V@
431AHVBOL51	SMT MB AH791 EH5LW I38145U22 230 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VHYNe/NC10@/CNV1@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4@/15@/15DIS@/FP3V@
431AHVBOL52	SMT MB AH791 EH5LW I58265U42 230 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VHYNe/NC10@/CNV1@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4@/15@/15DIS@/FP3V@
431AHVBOL53	SMT MB AH791 EH5LW I38145U22 230V8 HDMI	8145U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VSAM@/NC10@/CNV1@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4@/15@/15DIS@/FP3V@
431AHVBOL54	SMT MB AH791 EH5LW I58265U42 230V8 HDMI	8265U@/PCB@/WHL@/MEM@/SDP@/X76DHYNe/VGA@/G0@/X76VSAM@/NC10@/CNV1@/NCHG@/NRD@/3S@/LPC@/CMC@/255@/DVT@/X4@/15@/15DIS@/FP3V@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.05VALW_PRIM	+1.05V Always power rail	ON	ON	ON*1
+1.05V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.05VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VSDGPU	+1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON*2	OFF	OFF

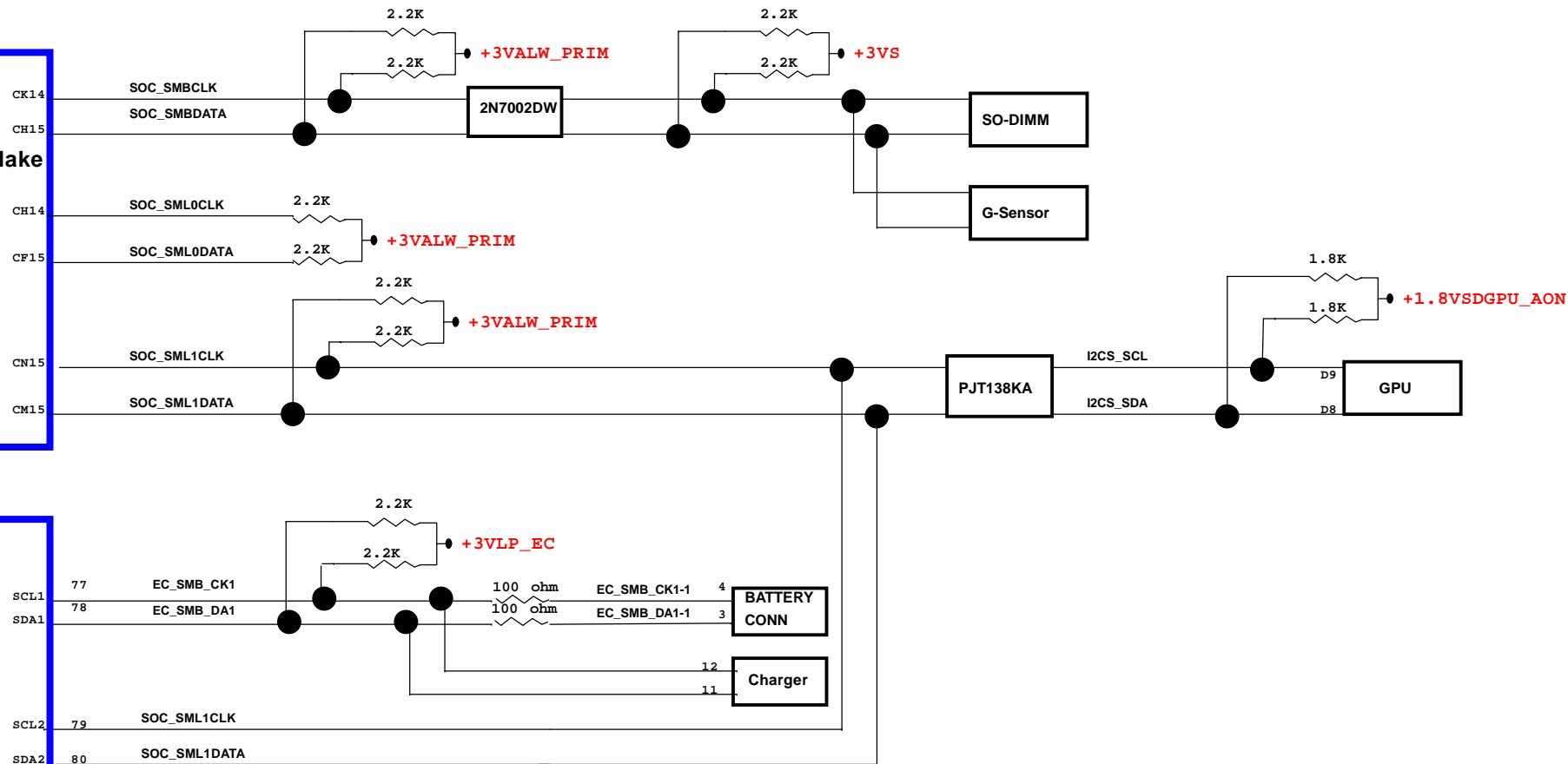
Note : ON\*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.  
ON\*2 power plane is ON when DGPU turn on



	Re
--	----

Whiskeylake  
SOC

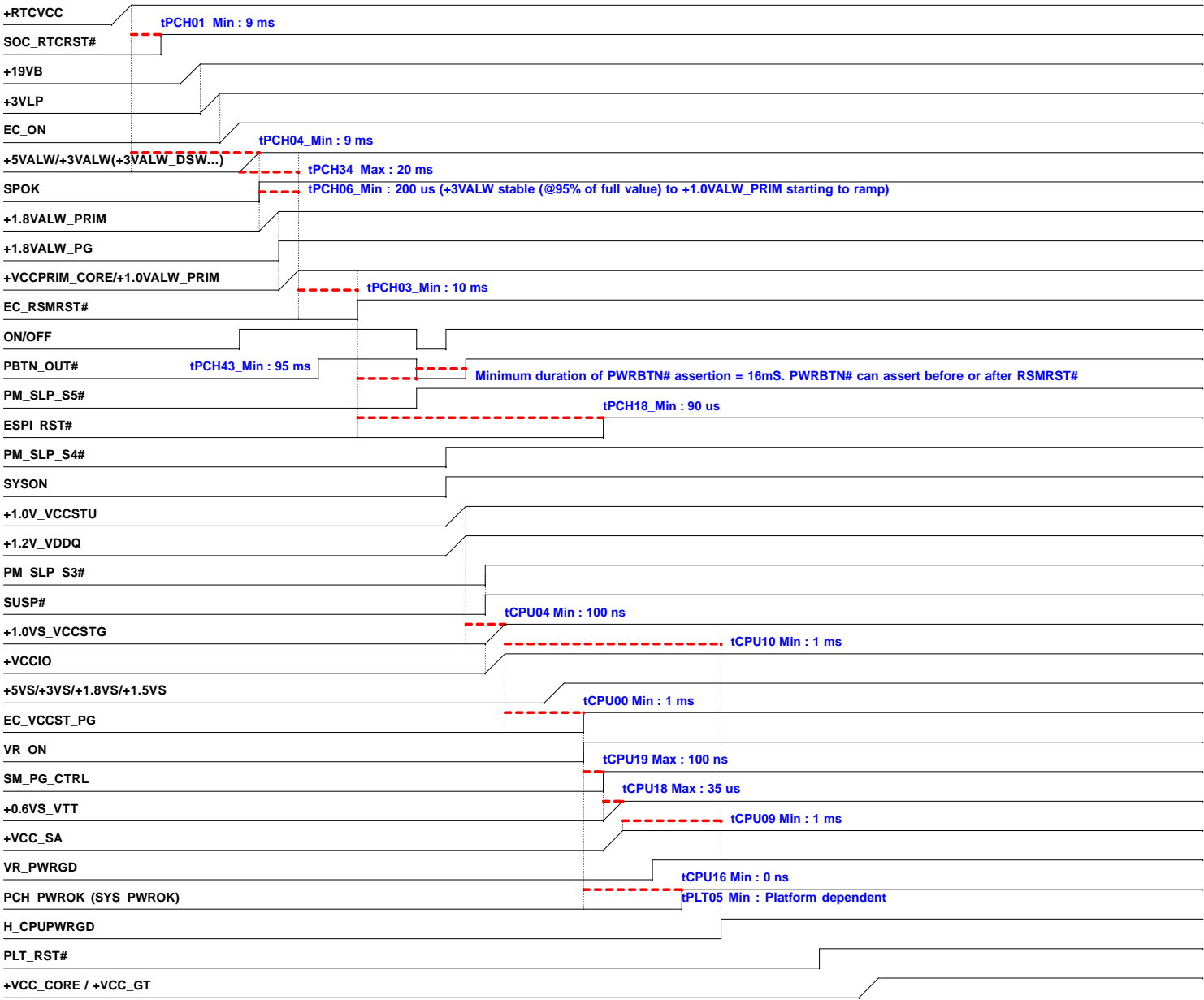
KBC  
KB9022



I2C Address Table

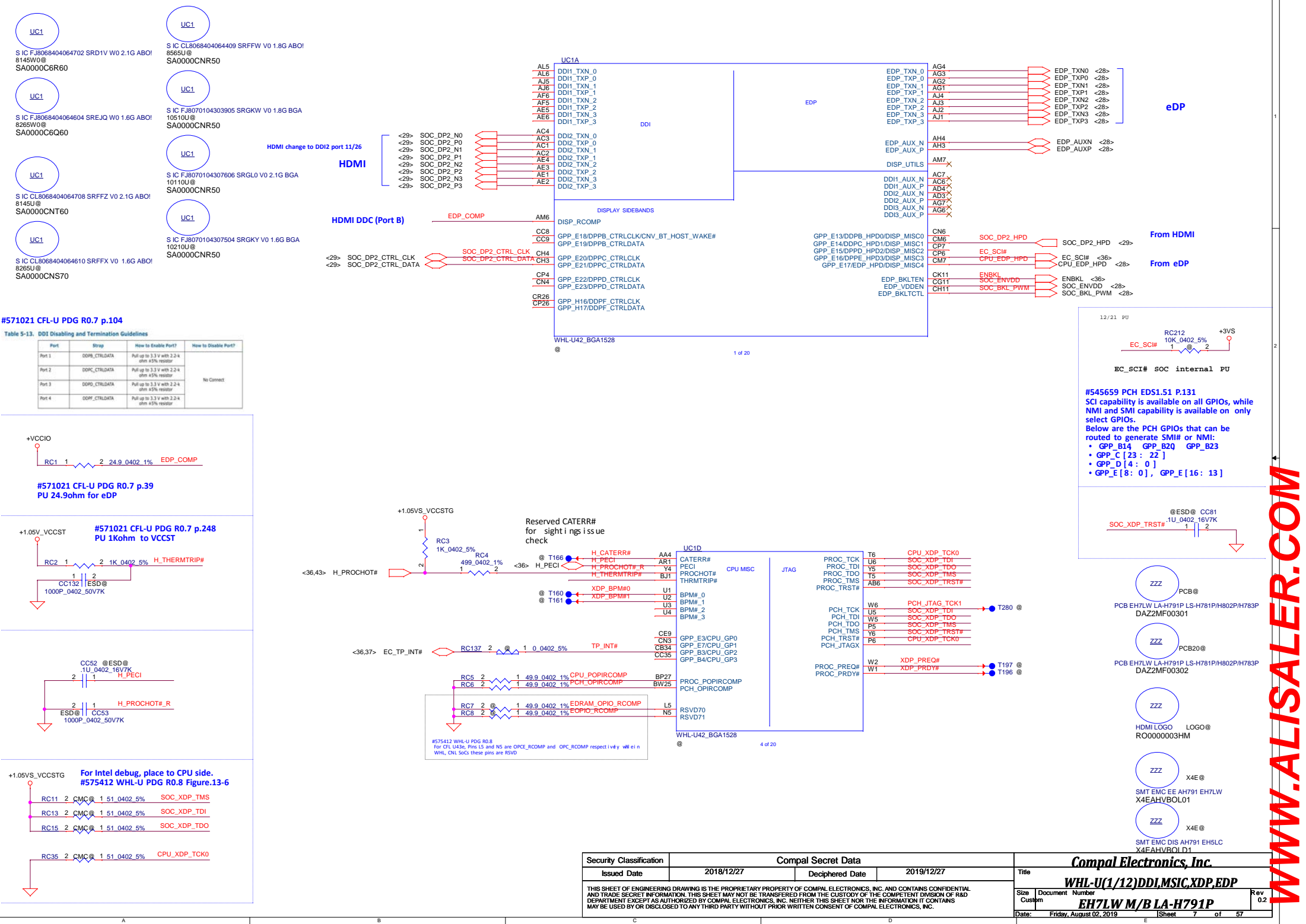
BUS	Device	Address (8 bit)
I2C_0 (+3VS)	Reserved	
I2C_1 (+3VALW_PRIM)	TM-P3393-003 (TP)	0x2C
	FA577E-1206 (TP-ELAN)	0x15
	SA577C-12A0 (TP-ELAN)	0x15
SOC_SMBCLK (+3VS)	SO-DIMM2	0xA4
	G-Sensor	0x30
SOC_SML1CLK (+3VALW_PRIM)	GPU	0x9E
	EC	
EC_SMB_CK1 (+3VLP)	BQ24781 (Charger IC)	0x12
	BATTERY PACK	0x16

PWR Sequence\_SKL-U2+2\_DDR3L\_Value\_NON CS



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Power Sequence	
Size	Document	Number	Rev	EH7LW M/B LA-H791P	
Custom				0.2	
Date:	Thursday, June 06, 2019	Sheet	6	of 57	

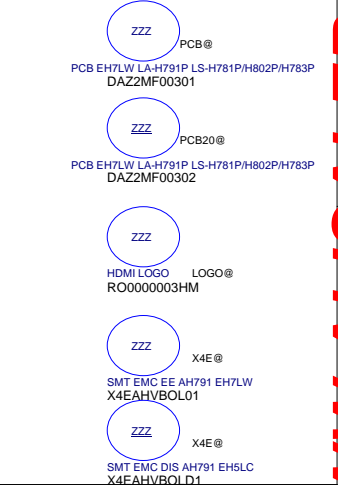
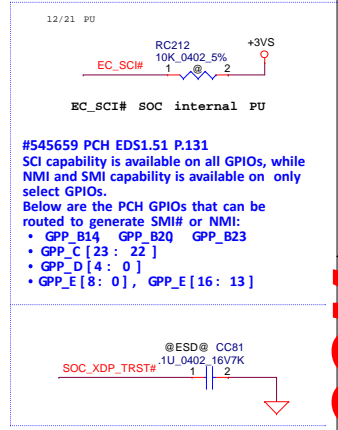
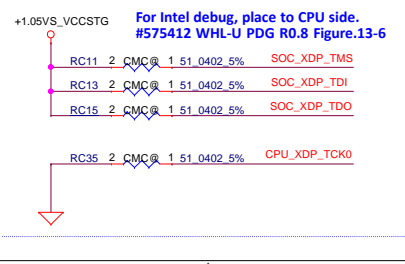
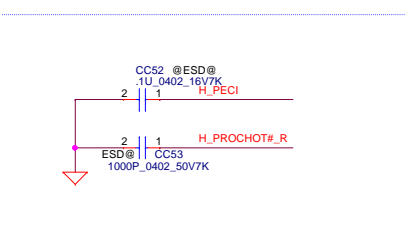
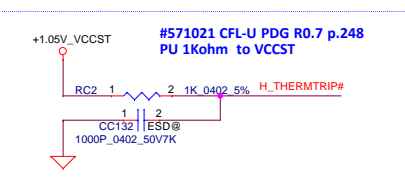
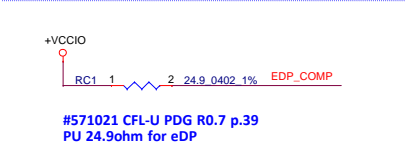
WWW.ALISALER.COM



#571021 CFL-U PDG R0.7 p.104

Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm 45% resistor	

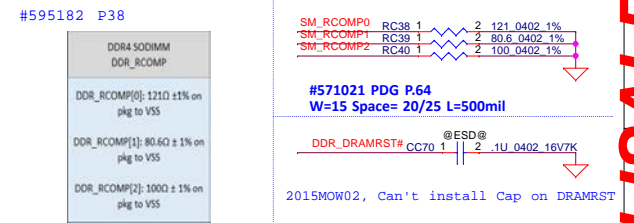
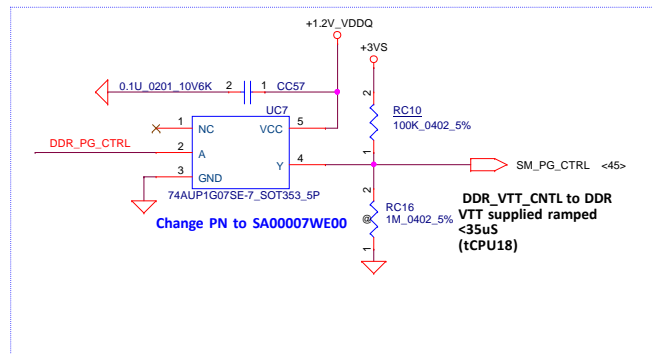
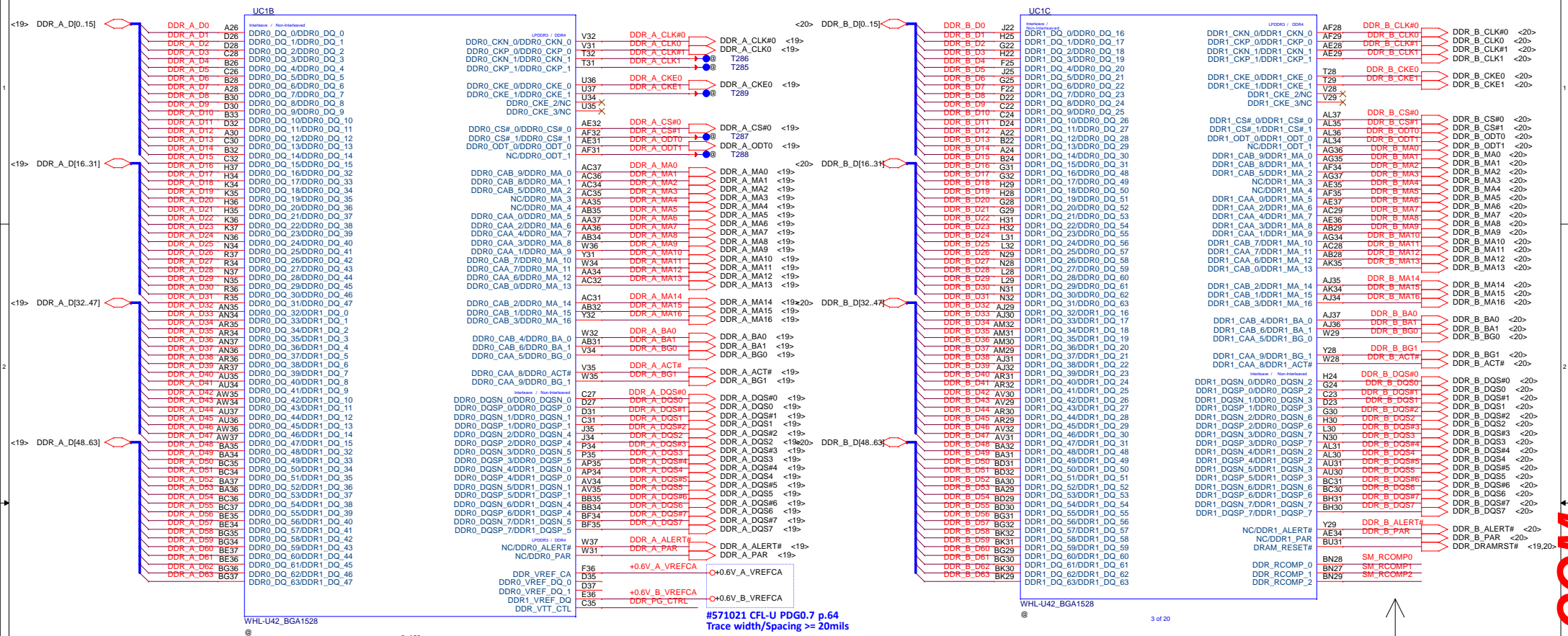


Security Classification		Compal Secret Data		Title	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(1/12)DDI,MSIC,XDP,EDP	
Size	Document	Number	Rev	EH7LW M/B LA-H791P	
Date:	Friday, August 02, 2019	Sheet	7 of 57		

WWW.ALISALER.COM

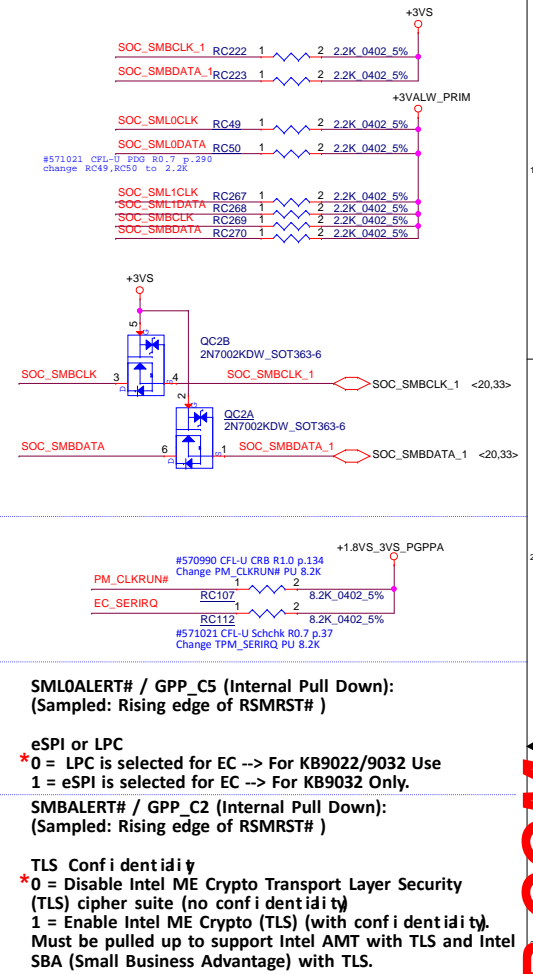
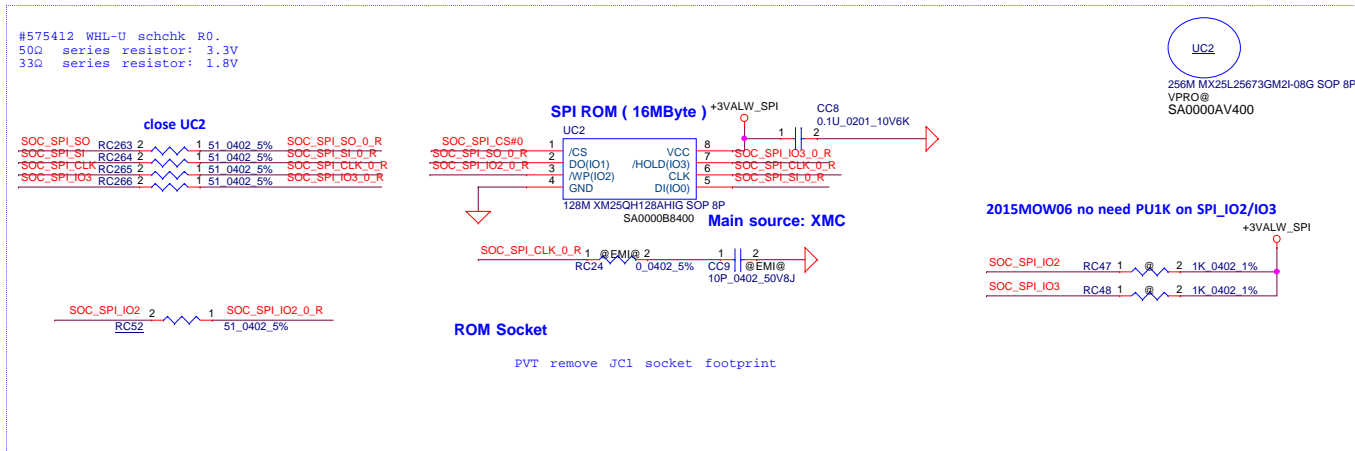
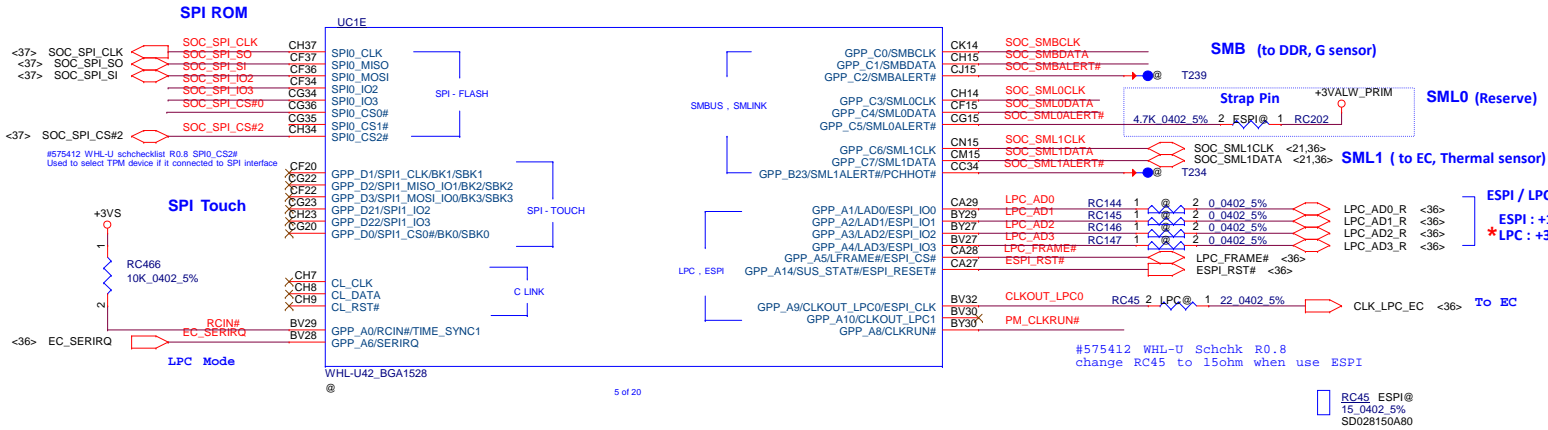


# Interleaved Memory



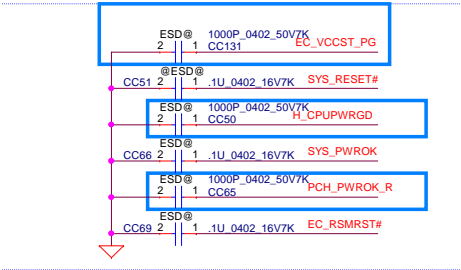
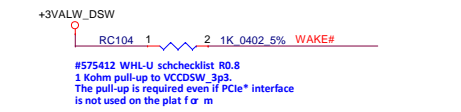
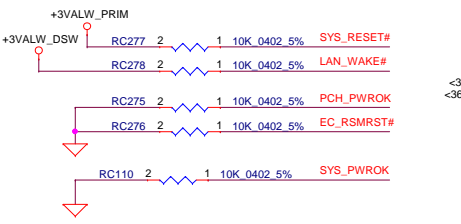
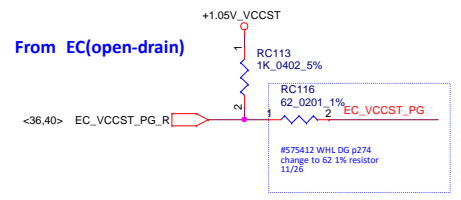
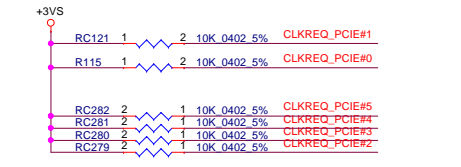
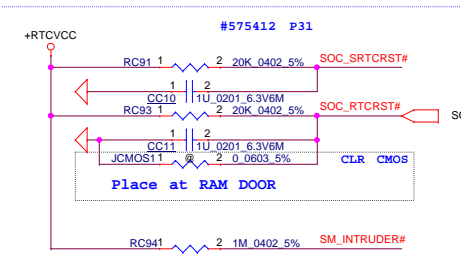
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>WHL-U(2/12)DDR4</b>			
Issued Date		2018/12/27		Deciphered Date		2019/12/27	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		<b>WHL-U(2/12)DDR4</b> <b>EH7LW M/B LA-H791P</b>	
				Size		Document Number	
				Custor		Rev 0.2	
				Date:		Thursday, June 06, 2019	
				Sheet		8 of 57	





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	WHL-U(3/12)SPI,ESPI,SMB,LPC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom	0.2
				Document Number	EH7LW M/B LA-H791P
				Date:	Thursday, June 06, 2019
				Sheet	9 of 57

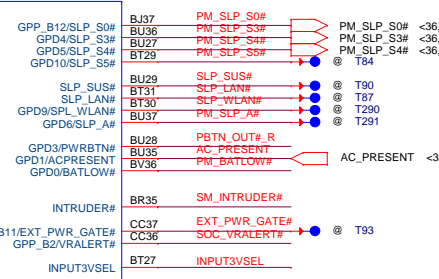
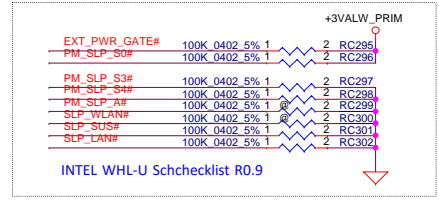
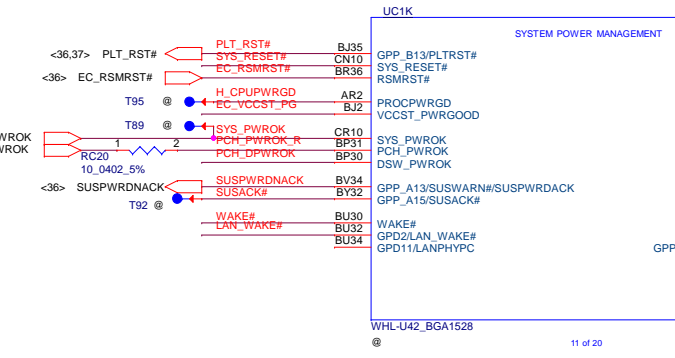
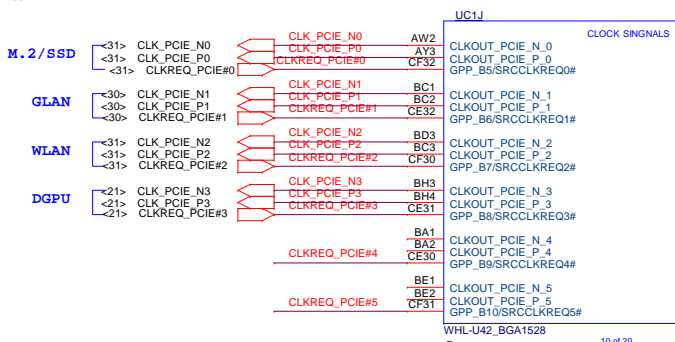
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	<b>WHL-U(4/12)HDA,EMMC,SDIO,CNV</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	<b>M/B LA-H791P</b>	<b>02</b>
				Date:	Thursday, June 06, 2019	Sheet 10 of 57



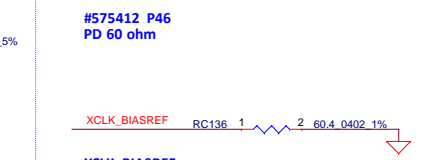
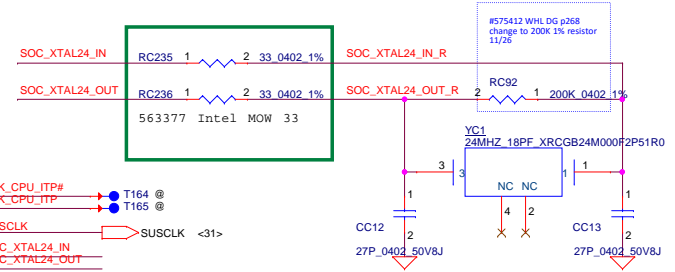
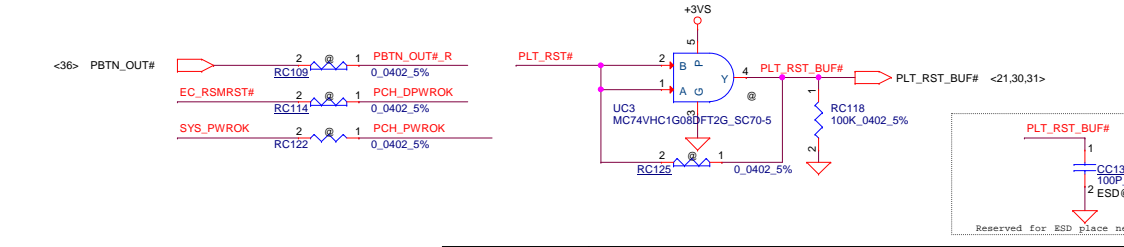
#543016 PDG2.0 P.599

PROCWPRGD is used only for power sequence debug and is not required to be connected to anything on the plat f or m

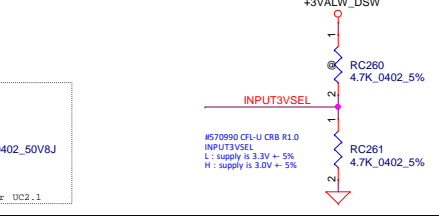
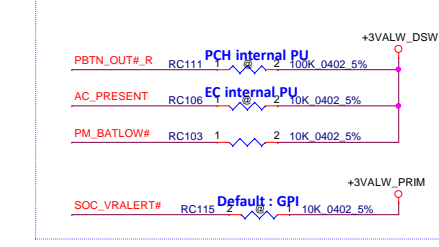
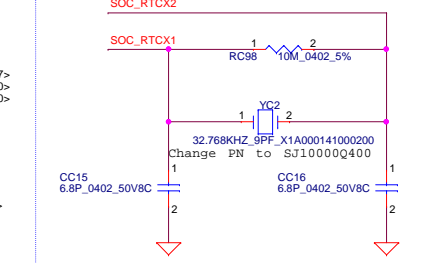
For layout routing ,PCIE CLK P0/P3 exchange



### PCH PLTRST Buffer

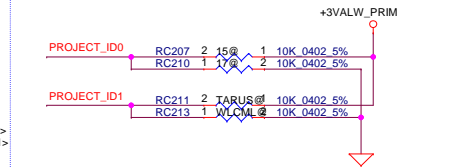
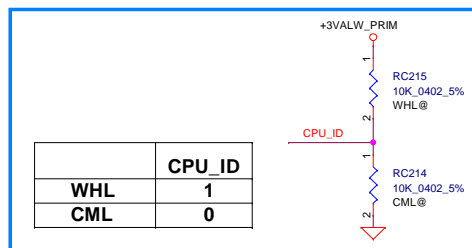
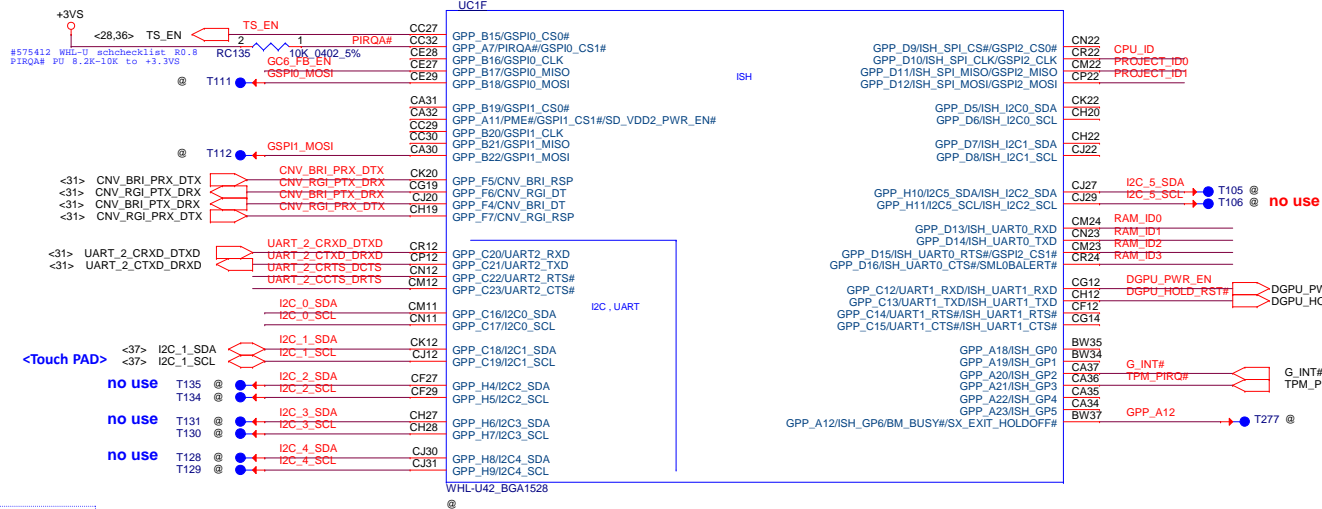


2014MOW48: Skylake-U use 24M 50 ohm ESR Cannonlake-U use 38.4M 30 ohm ESR

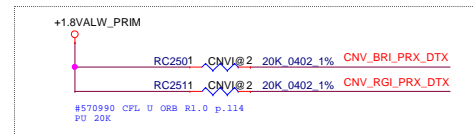
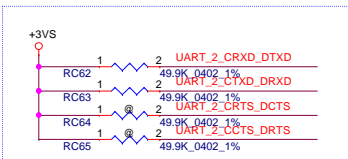


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(5/12)CLK,GPIO	
Size	Custom	Document Number	EH7LW M/B LA-H791P	Rev	0.2
Date:	Thursday, June 06, 2019	Sheet	11	of	57

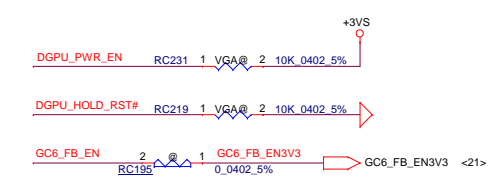
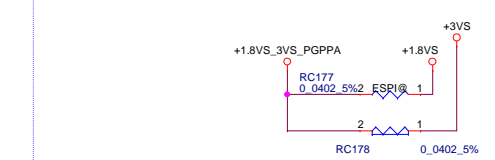
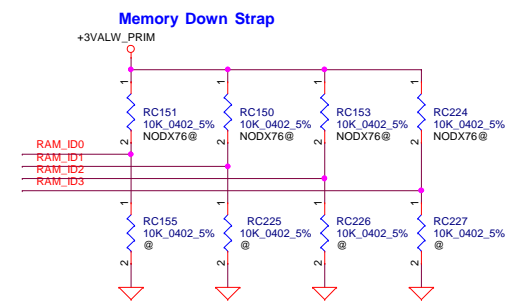
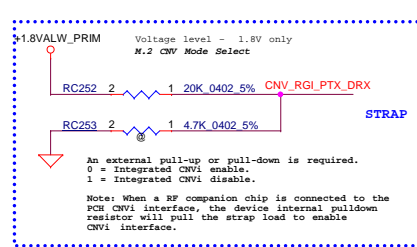
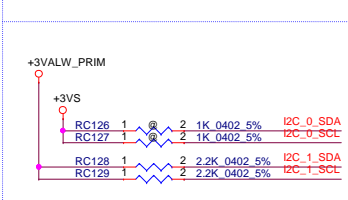
WWW.ALISALER.COM



Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* EH7LW/FH7LC	0	0
EH5LW/FH5LC	0	1
NA	1	0
FH5TW	1	1



6 of 20



## Functional Strap Definitions

**GSPI0\_MOSI / GPP\_B18 (Internal Pull Down):**  
(Rising edge of PCH\_PWROK)  
No Reboot

- \* 0 = Disable No Reboot mode. --> AAX05 Use
- 1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

**GSPI1\_MOSI / GPP\_B22 (Internal Pull Down):**  
(Rising edge of PCH\_PWROK)

**Boot BIOS Strap Bit**  
\* 0 = SPI Mode --> AAX05 Use  
1 = LPC Mode

Z2Z1	Hynix4GB	X76DHYN@	X76829BOL04
Z2Z2	Micron4GB	X76DMIC@	X76829BOL05
Z2Z3	Samsung4GB	X76DSAM@	X76829BOL06

	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000BMN30 (S IC D4 512M16 H5AN8G6NCR-VKC FBGA ABOI)
Micron 4GB	0	0	0	1	SA0000ARD60 (S IC D4 8G/2666 MT40A512M16LY-075:E ABOI)
Samsung 4GB	0	0	1	0	SA0000B6F00 (S IC D4 512M16 K4A8G165WC-BCTD FBGA 96P)
No OnBoard Memory	1	1	1	1	No On Board Memory

Security Classification	Compal Secret Data		Title	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	WHL-U(6/12)GPIO
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom
				Document Number EH7LW M/B LA-H791P
				Rev 0.2
				Date: Thursday, June 06, 2019
				Sheet 12 of 57

WWW.ALISALER.COM

11/28  
For layout routing  
PCIE P5/P6 exchange

NGFF WLAN+BT(Key E)

GLAN

HDD

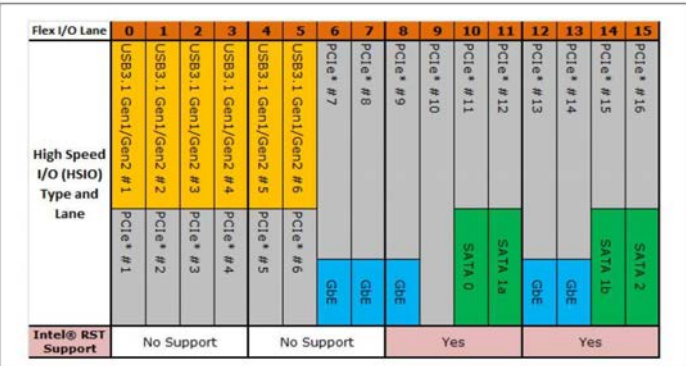
ODD

NGFF SSD(Key M)

(Need Lane Reversal)

### 6.1.2.1 Cannon Lake U (CNL U) PCH-LP

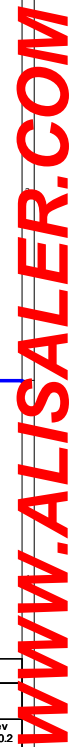
Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

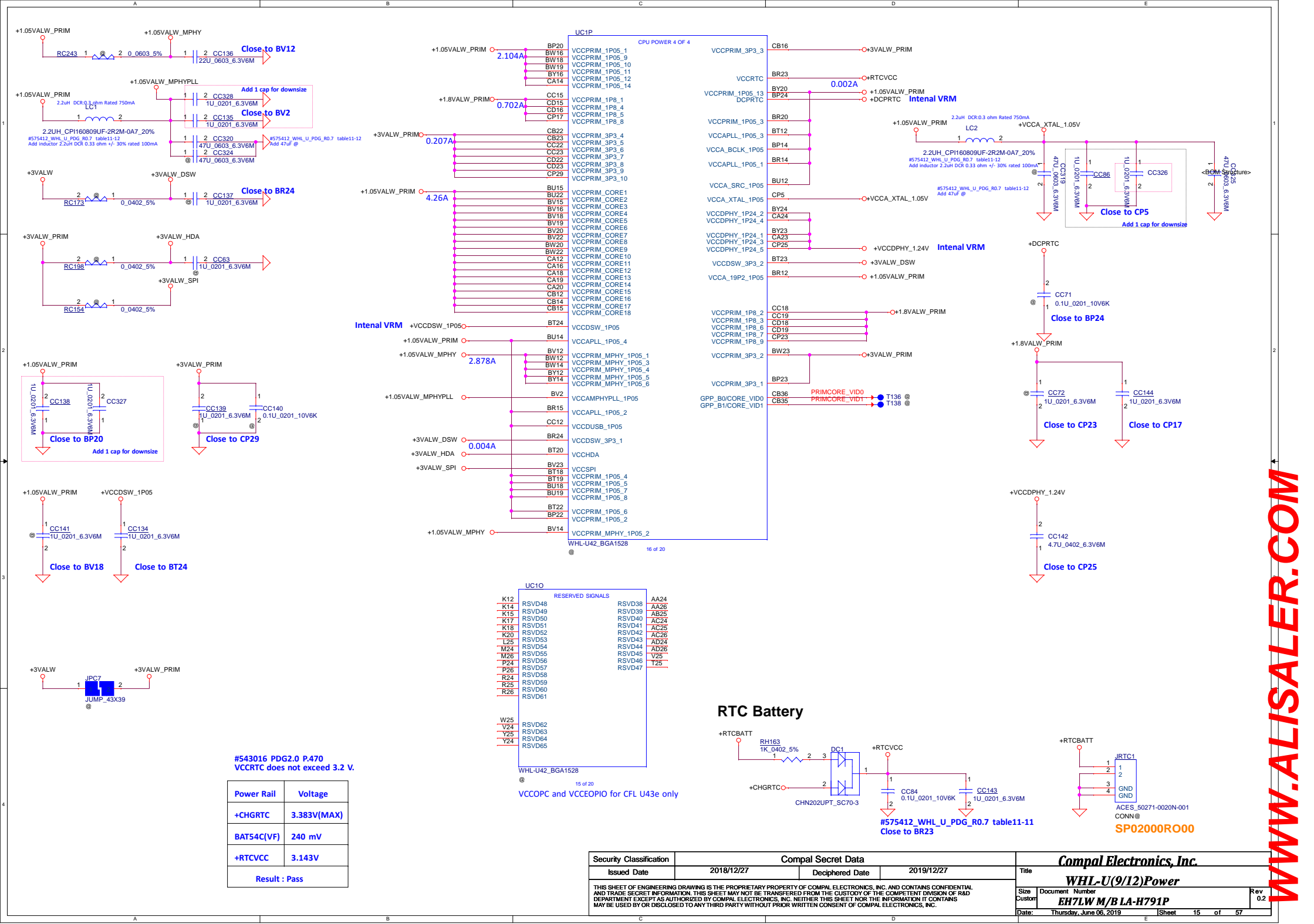


GPIO	DEVICE CONTROL
USB_OC#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

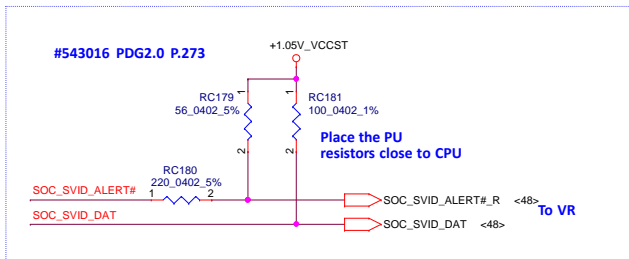
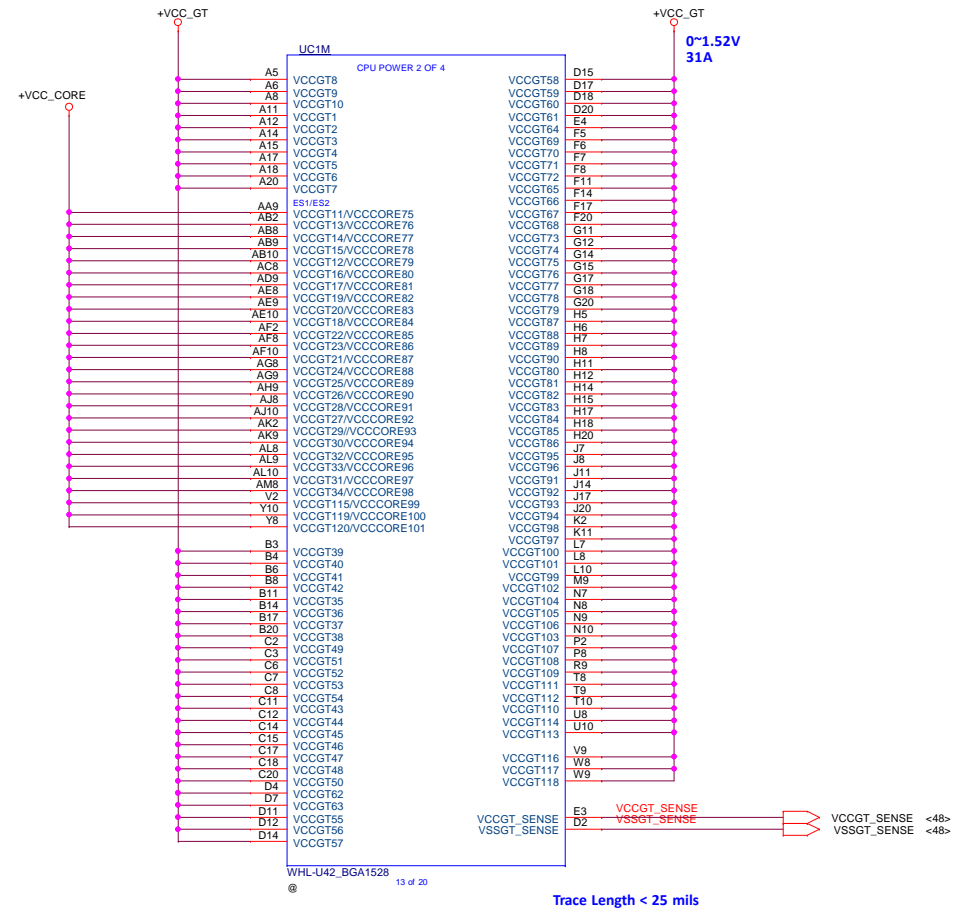
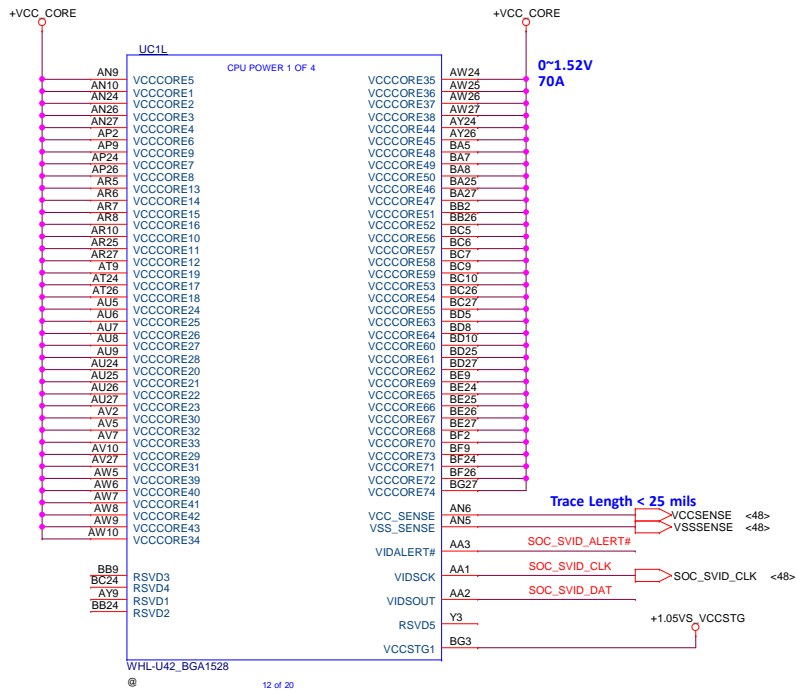
WWW.ALISALER.COM







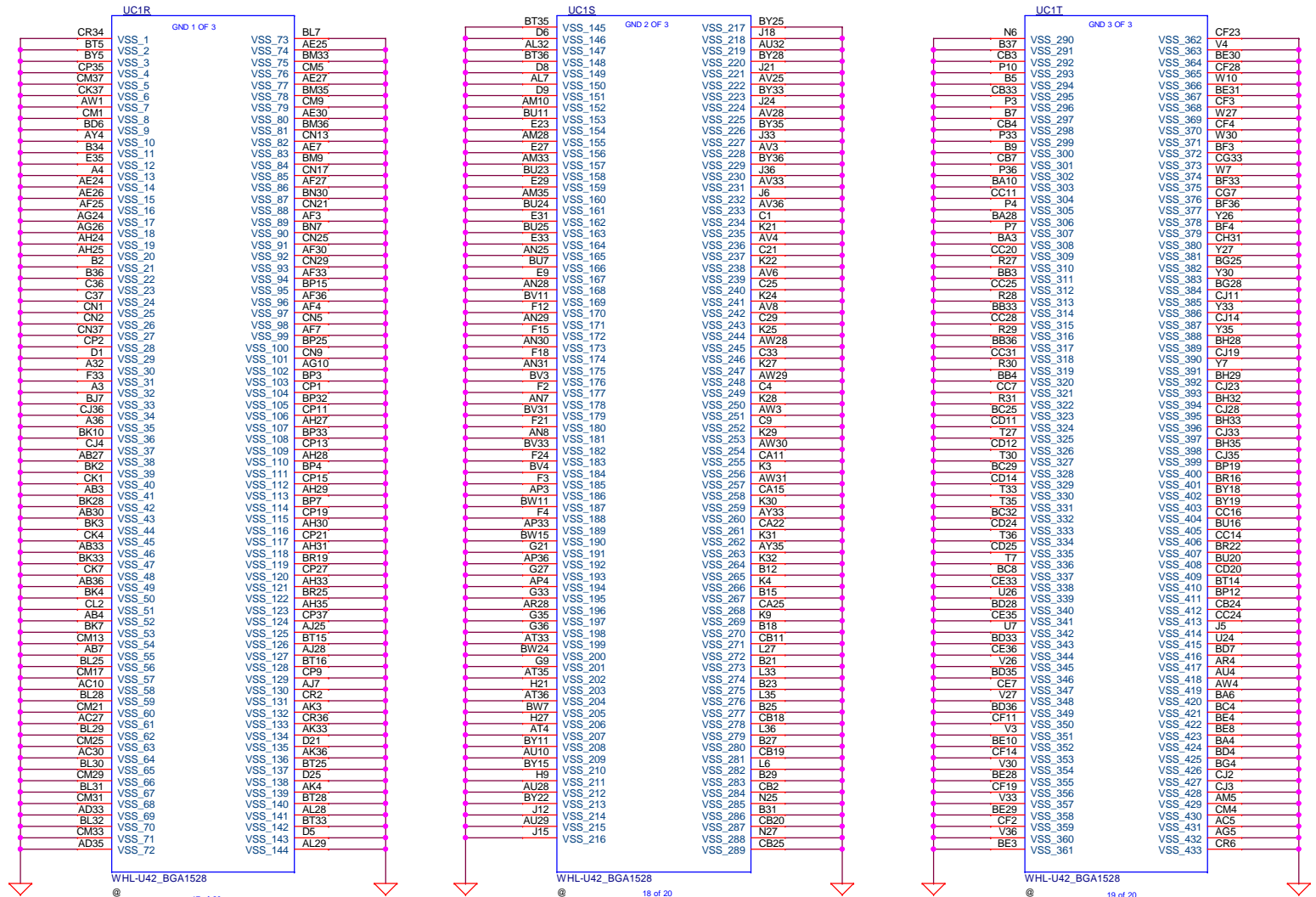


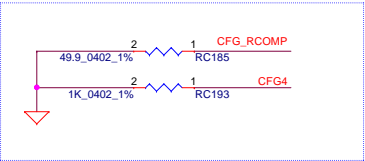
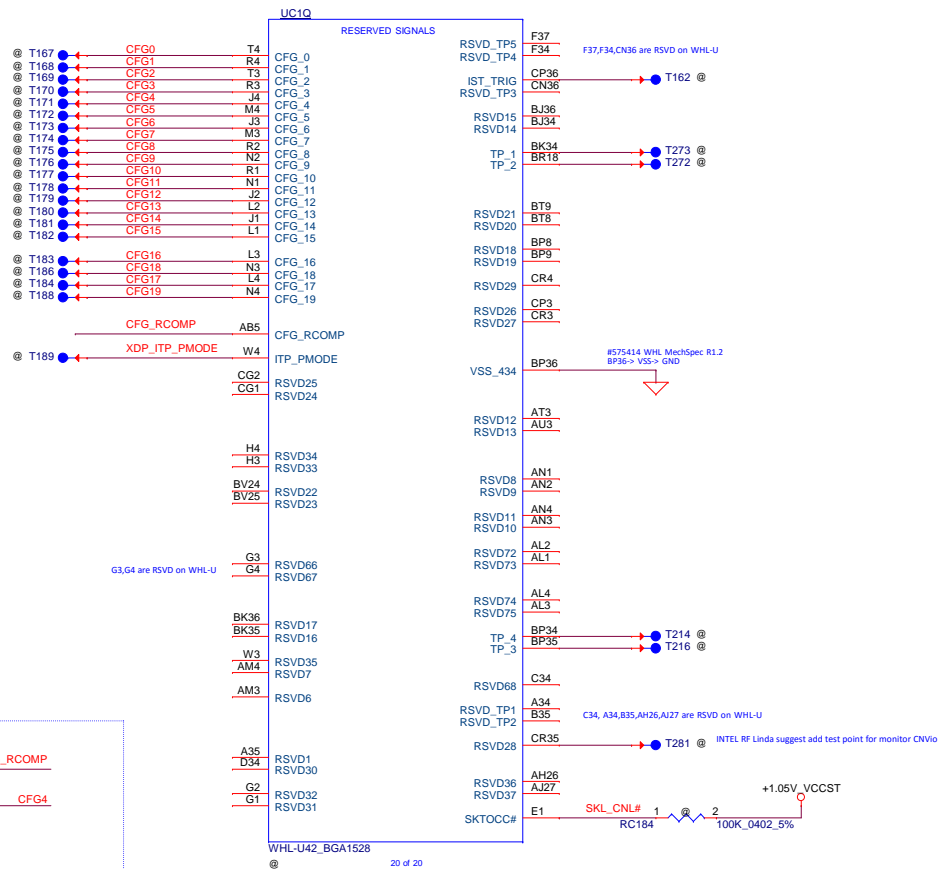


#### Processor Power Rails

Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_LPB</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCIOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Security Classification		Compal Secret Data		Title	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(10/12)Power,SVID	
Size	Document	Number	Rev	EH7LW M/B LA-H791P	
Date:	Thursday, June 06, 2019	Sheet	16	of 57	





#### Display Port Presence Strap

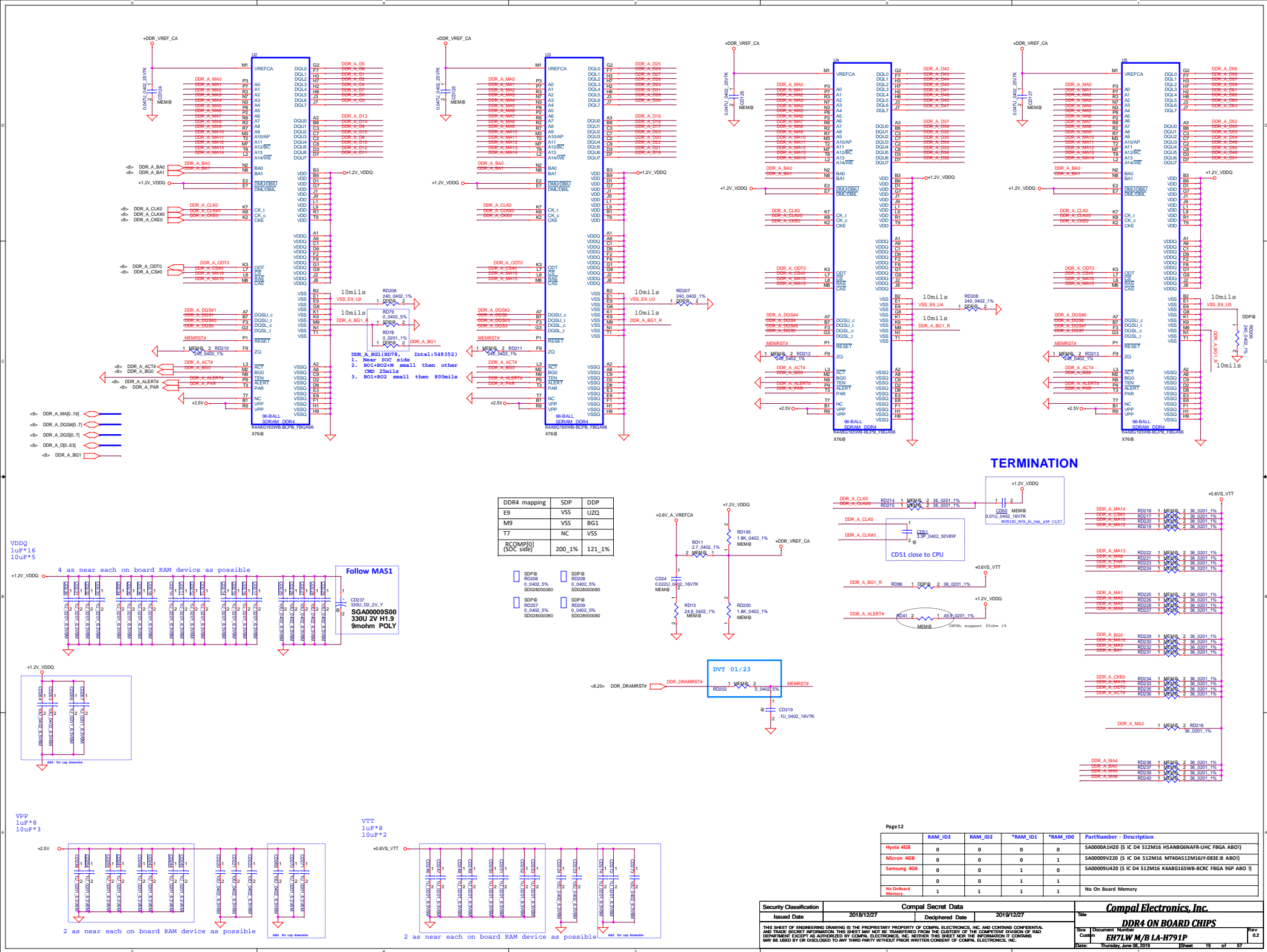
CFG4

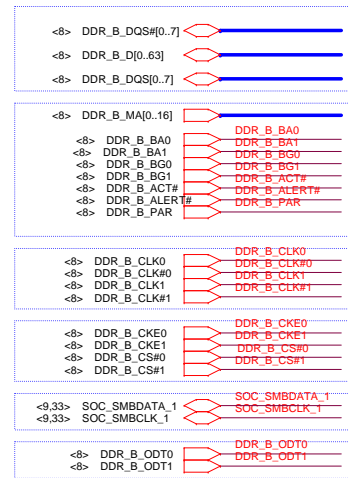
1 : Disabled; No Physical Display Port  
at tached to E mbedded D splay Port

0 : Enabled; An external Display Port device is  
connected to the Embedded Display Port

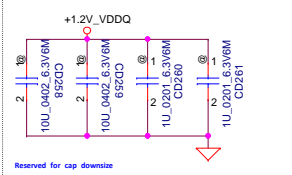
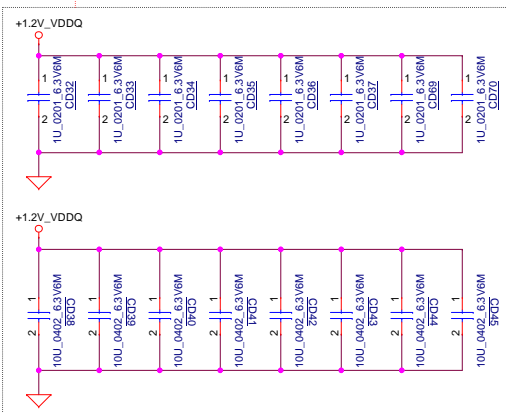
#544669 CRB1.1 P54  
#544924 SKL EDS1.2 P125  
PROC\_SELECT#  
This pin is for compatibility with future  
platforms. It should be unconnected for  
the processor.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(12/12)RSVD	
Size	Document	Number	Rev	Date: Thursday, June 06, 2019	
Custom	EH7LW M/B LA-H791P		0.2	Sheet 18 of 57	

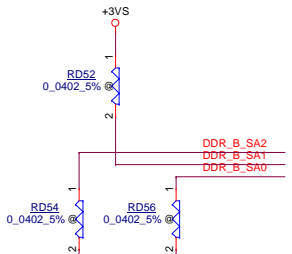
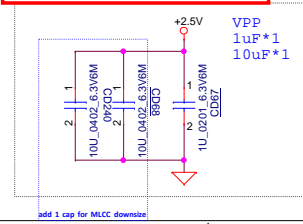




Layout Note:  
Place near JDIMM2



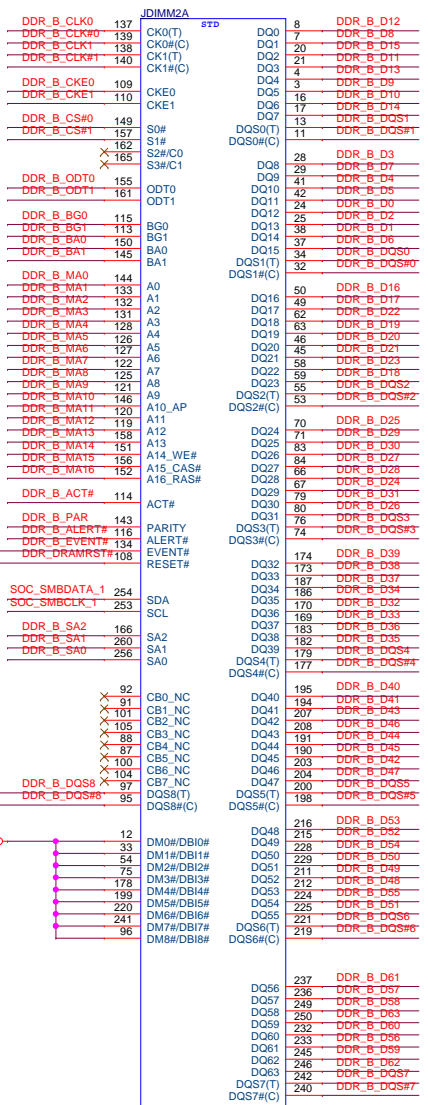
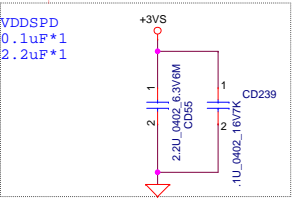
Layout Note:  
Place near JDIMM1.257,259



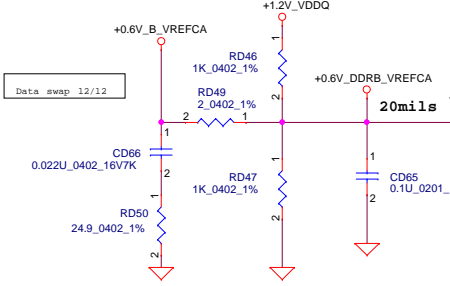
VDDQ  
1uF\*8  
10uF\*8  
330uF\*1

Layout Note:  
Place near JDIMM2.255

#575412 WHL-U PDG R0.7 Table 4-23  
add 0.1uF

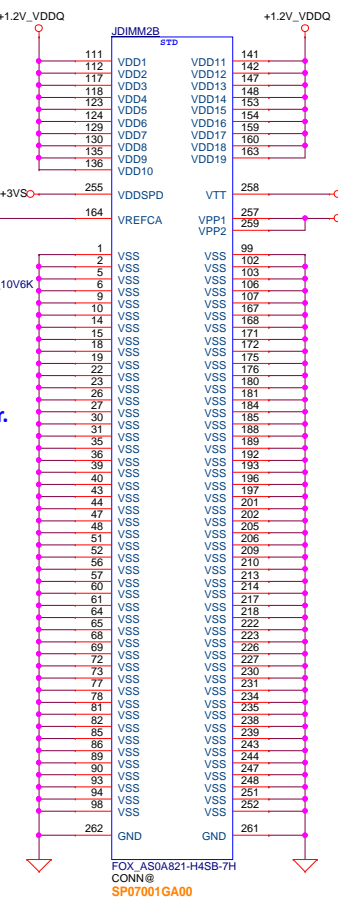


Compatible with SP07001HW00

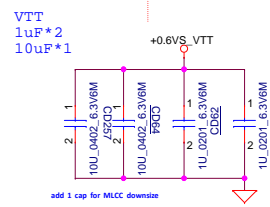


Place near to SO-DIMM connector.

Standard Type  
2-3A to 1 DIMMs/channel



Layout Note:  
Place near JDIMM1.258

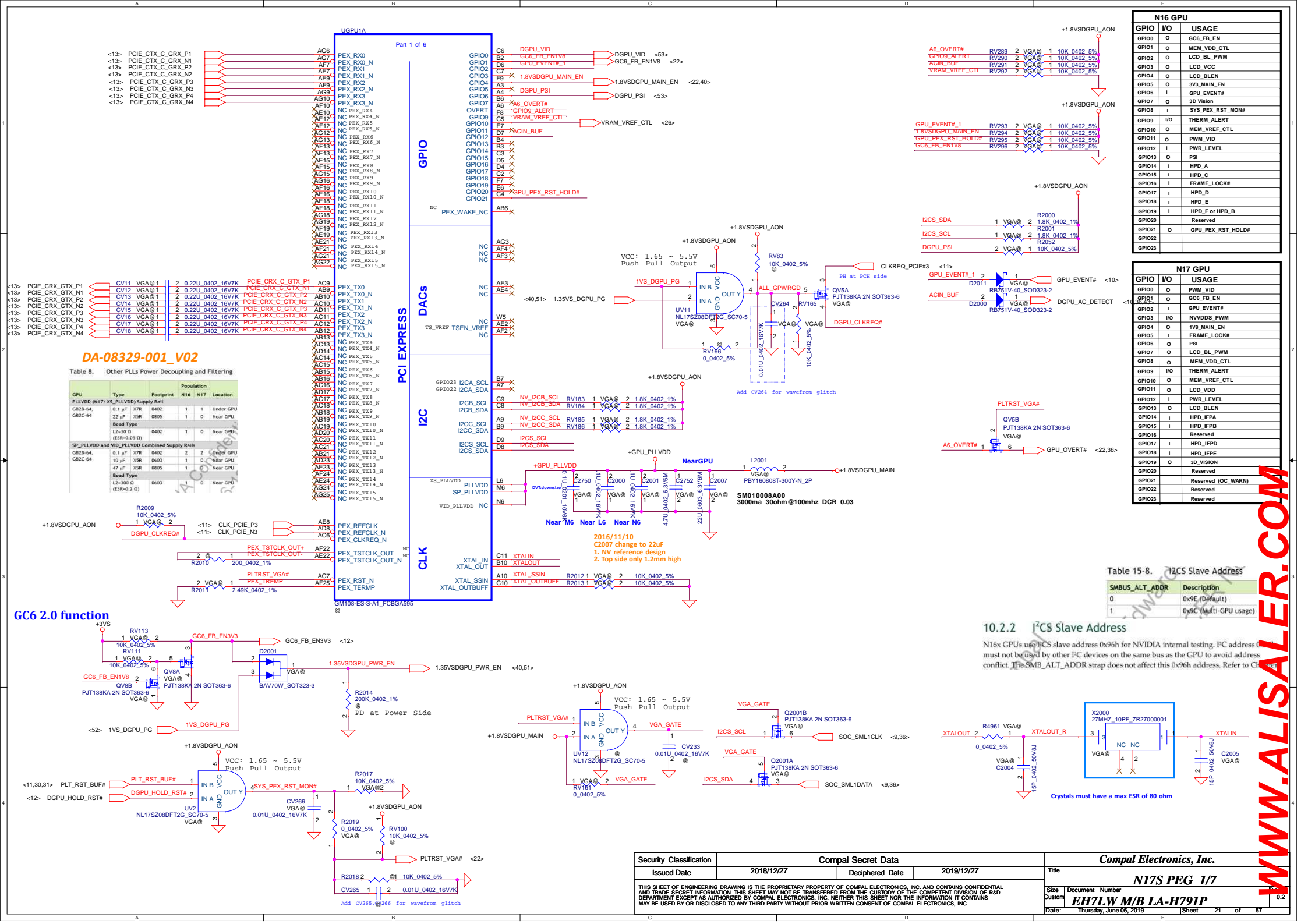


Security Classification		Compal Secret Data	
Issued Date	2018/12/27	Deciphered Date	2019/12/27
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			

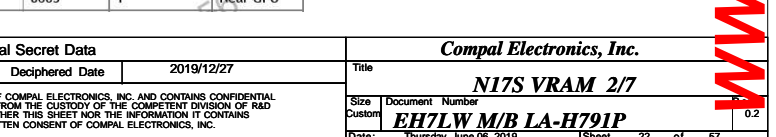
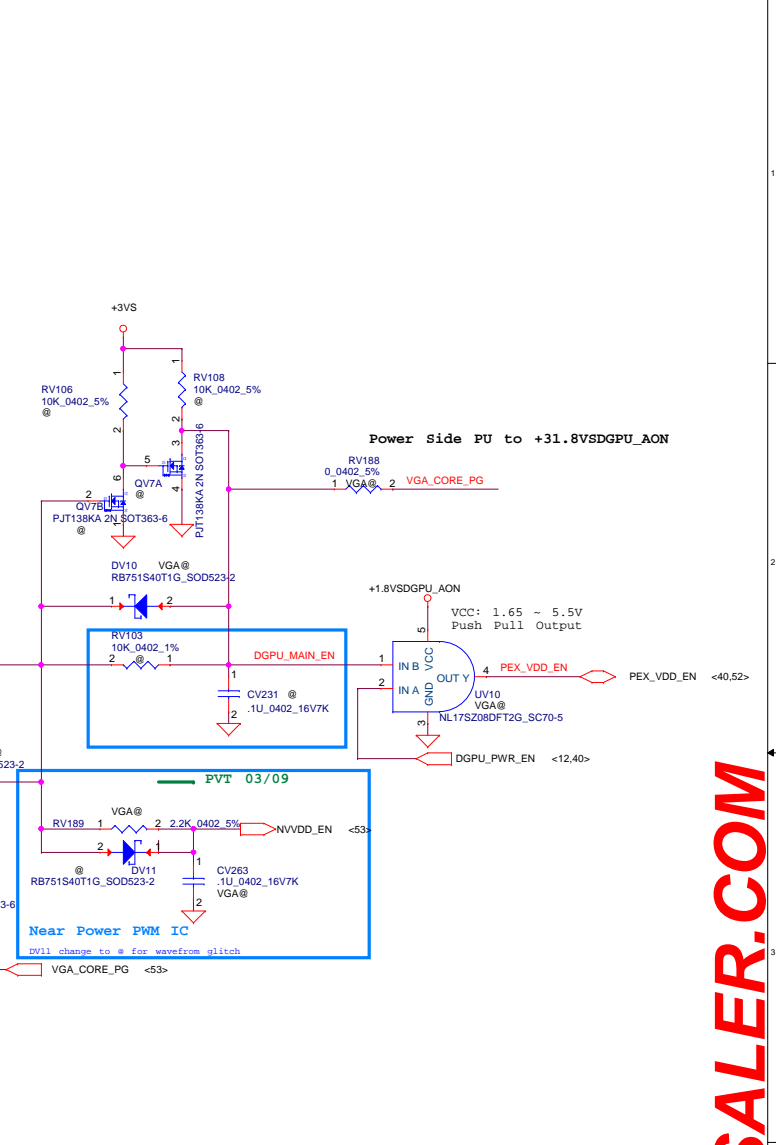
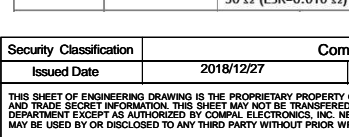
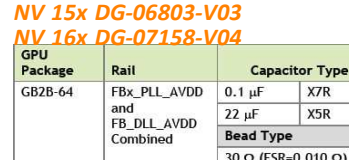
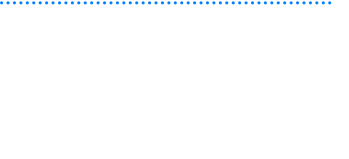
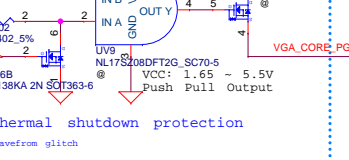
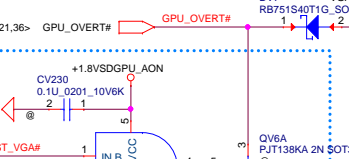
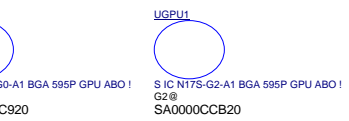
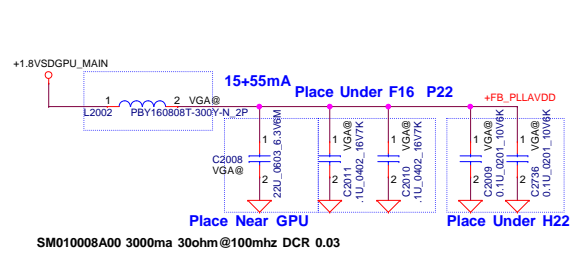
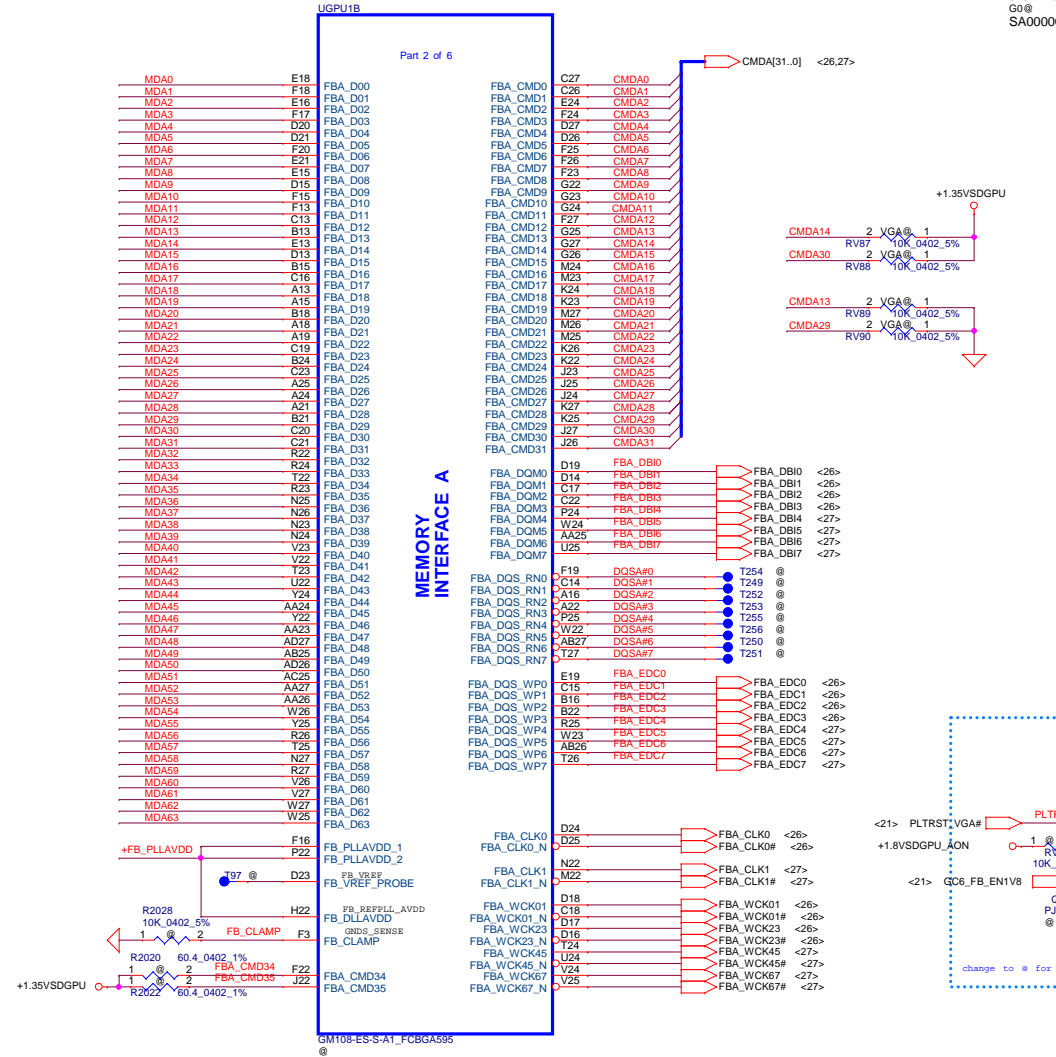
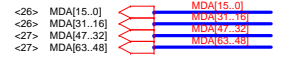
Title			
DDR4 DIMMB			
Size	Document Number	Rev	
Custom	EH7LW M/B LA-H791P	0.2	
Date:	Thursday, June 06, 2019	Sheet	20 of 57

WWW.ALISALER.COM





VRAM Interface



NV 15x DG-06803-V03  
NV 16x DG-07158-V04

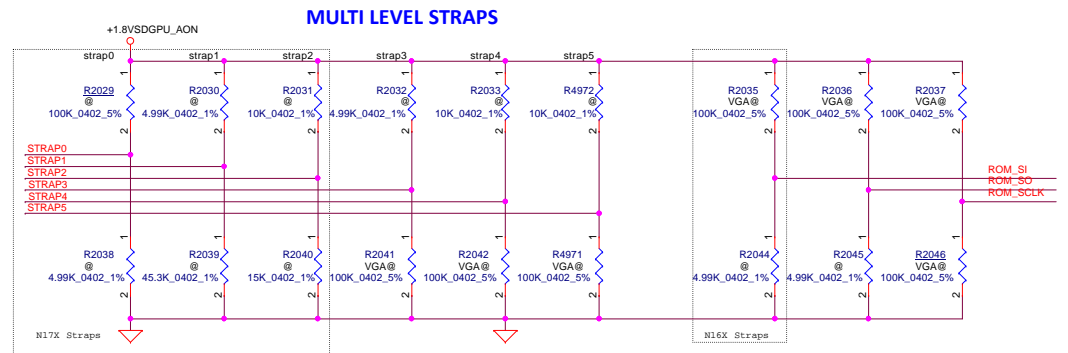
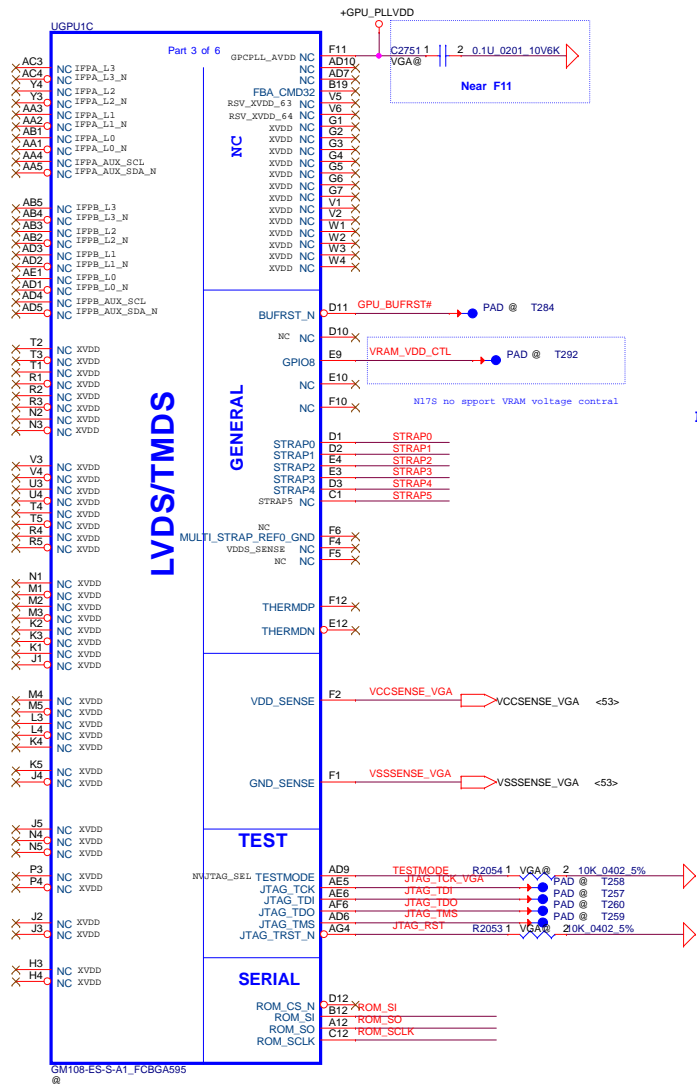
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD	0.1 µF	X7R	0402	2
	FBx_WCK01_N	22 µF	X5R	0805	1
	FBx_WCK23_N	30 Ω	0603	1	1

Security Classification	Compal Secret Data
Issued Date	2018/12/27
Deciphered Date	2019/12/27

Compal Electronics, Inc.	
Title	
N17S VRAM 2/7	
Size	Document Number
Custom	EH7LW M/B LA-H791P
Date:	Thursday, June 06, 2019
Sheet	22 of 57

WWW.ALISALER.COM

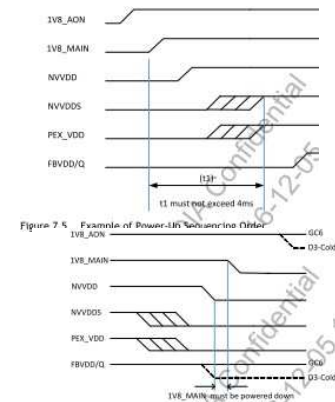




Multi strap table

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N17S-G0	+1.35V	sr	X76xxxxxxx	3.0GHz	256Mx32x2 ZG	0x4 (SA00009TV50) Micron MT51J256M32HF-70-B	PD 100K	PD 100K	PU 100K						
N17S-G2						0x5 (SA00009U160) Hynix H5GC8H24AJR-ROC	PU 100K	PD 100K	PU 100K						
						0x0 (SA00009TA10) Samsung K4G80325FB-HC25	PD 100K	PD 100K	PD 100K						
							PD 100K	PD 100K	PD 100K						
							PD 100K	PU 100K	PD 100K						
							PU 100K	PD 100K	PD 100K						

NV 17S DG-07785-001\_V07



DA-08329-001\_V02

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population	N16	N17	Location
PLLVD0 (N17: XS_PLLVD0) Supply Rail						
GB2B-64	0.1 µF	X7R 0402	1	1	Under GPU	
GB2C-64	22 µF	XSR 0805	1	0	Near GPU	
	Bead Type					
	L2=30 Ω	0402	1	0	Near GPU	
	(ESR=0.05 Ω)					
SP_PLLVD0 and VID_PLLVD0 Combined Supply Rails						
GB2B-64	0.1 µF	X7R 0402	2	2	Under GPU	
GB2C-64	10 µF	XSR 0603	1	0	Near GPU	
	47 µF	XSR 0805	1	0	Near GPU	
	Bead Type					
	L2=300 Ω	0603	1	0	Near GPU	
	(ESR=0.2 Ω)					
HC (N17: GPCPLL_AVDD0) Supply Rail						
GB2B-64	0.1 µF	X7R 0402	N/A	1	Under GPU	
	4.7 µF	X6S 0603	N/A	1	Near GPU	
	22 µF	X6S 0805	N/A	1	Near GPU	
	Bead Type					
	L=90 Ω	0603	N/A	1	Near GPU	
	(ESR=0.010 Ω)					

# NV 16x DG-07158-V05

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

# DA-08329-001\_V02

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

# NV 16x DG-07158-V05

Table 3-16. PEX\_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

# NV 16x DG-07158-V05

Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR5/BGA-170	1.35V or 1.50V	40.2Ω	40.2Ω	60.4Ω

# NV 16x DG-07158-V05

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU

# DA-08329-001\_V01

Table 9. VDD AON and VDD\_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
N16 3V3_MAIN (N17 VDD18) Supply Rail					
GB2B-64, GB2C-64	0.1µF	X7R	0402	2	2
	1.0µF	X6S	0603	1	1
	4.7µF	X6S	0603	1	1
N16 3V3_AON (N17 VDD_AON) Supply Rail					
GB2B-64, GB2C-64	0.1µF	X7R	0402	1	1
	1.0µF	X6S	0603	1	1
	4.7µF	X6S	0603	1	1

# NV 16x DG-07158-V05

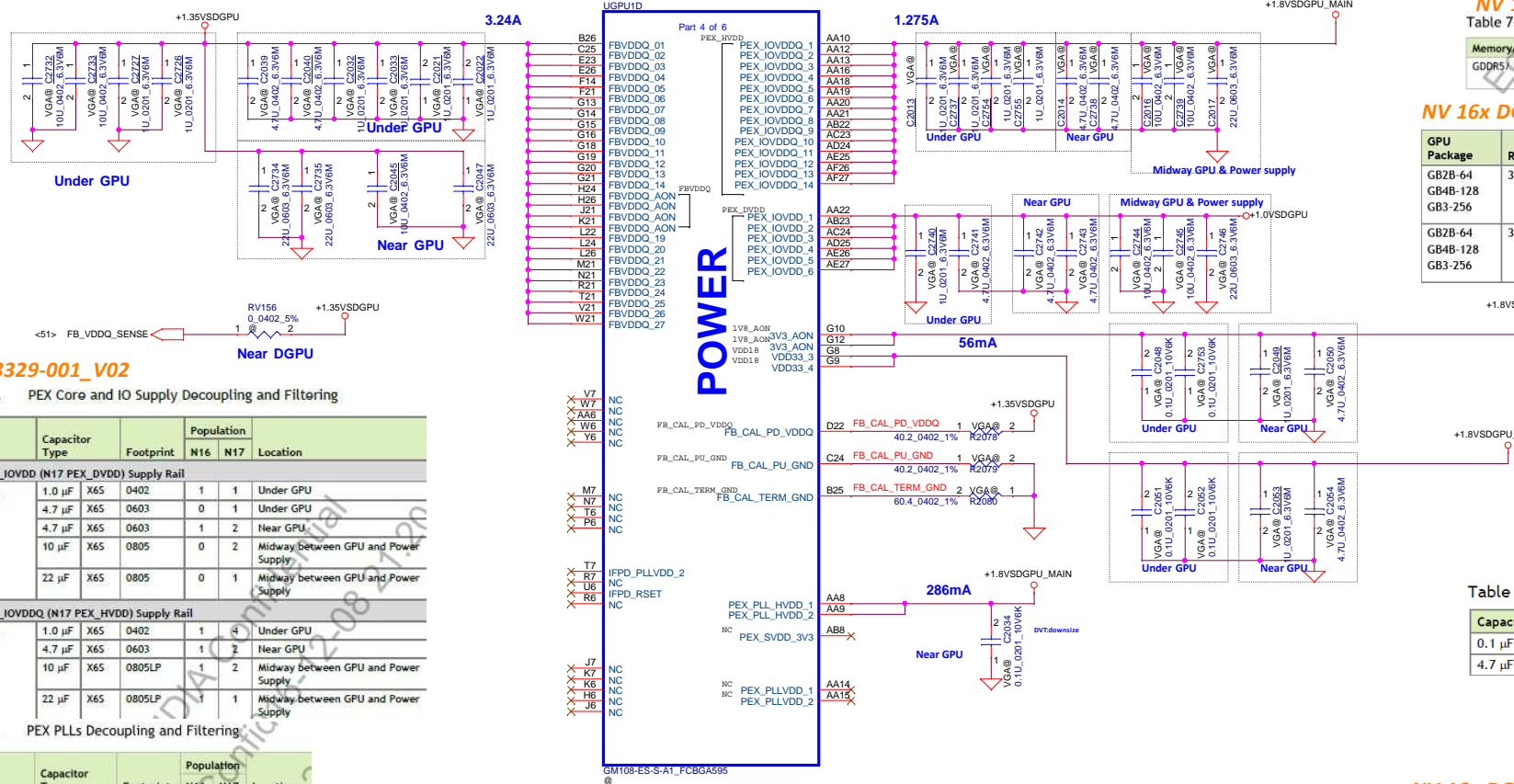
Table 3-18. PEX\_SVDD\_3V3 and PEX\_PLL\_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X7R	0402	1	Near GPU
4.7 $\mu$ F	X5R	0603	2	Near GPU

# NV 16x DG-07158-V05

Table 3-17. PEX\_PLLVDD Decoupling

Capacitor Type	Footprint	Population	Location	
0.1 $\mu$ F	X7R	0402	1	Under GPU
1.0 $\mu$ F	X5R	0603	1	Near GPU
4.7 $\mu$ F	X5R	0805	1	Near GPU



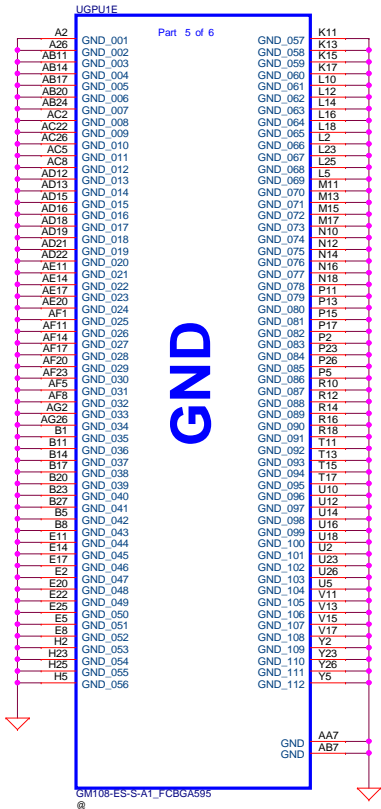
# DA-08329-001\_V02

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population		Location
				N16	N17	
PEX_PLLVDD Supply Rail						
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU



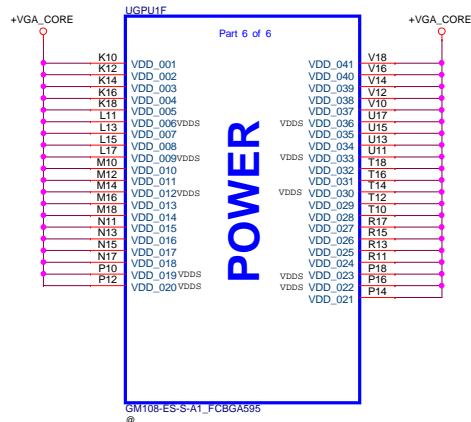
### SP-08318-001\_V03

Table 7. Output EDP-Continuous

	NVVD	GPU FBIO	FB Total <sup>1,2</sup>	1.0V Total <sup>1</sup>	1.8V Total <sup>2</sup>
	—	1.35V <sup>4</sup>	1.35V <sup>4</sup>	1.0V <sup>4</sup>	1.8V <sup>4</sup>
Product	(A)	(A)	(A)	(A)	(A)
N175-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

	NVVD	GPU FBIO	FB TOTAL <sup>4</sup>	1.0V Total <sup>1</sup>
	—	1.35V <sup>3</sup>	1.35V <sup>3</sup>	1.0V <sup>3</sup>
Product	(A)	(A)	(A)	(A)
N175-G1	60.1	3.2	6.6	0.2



### DA-08329-001\_V01

Table 3. NVVD and NVVDS Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location
NVVDD Supply Net					
GB2B-64, GB2C-64	4.7 $\mu$ F X6S	0603	10	8	Under GPU
	1 $\mu$ F X6S	0402	4	3	Under GPU
	47 $\mu$ F X5R	0805	1	-	Near GPU
	10 $\mu$ F X7R	0805	-	4	Near GPU
	22 $\mu$ F X5R	0805	1	3	Near GPU
	4.7 $\mu$ F X5R	0805	1	4	Near GPU
	330 $\mu$ F POS	7343	1	1	Near GPU
NVVDD5 Supply Net					
GB2C-64 Only	4.7 $\mu$ F X6S	0603	N/A	4	Under GPU
	1 $\mu$ F X6S	0402	N/A	2	Under GPU
	10 $\mu$ F X6S	0805	N/A	7	Near GPU
	22 $\mu$ F X6S	0805LP	N/A	1	Near GPU
	330 $\mu$ F POS	7343	N/A	1	Near GPU

### NV 16x DG-07158-V05

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64 / GB2-64	4.7 $\mu$ F X6S	0603	10	10	Under GPU
	1 $\mu$ F X6S	0402	4	4	Under GPU
	47 $\mu$ F X5R	0805	1	1	Near GPU
	22 $\mu$ F X5R	0805	1	1	Near GPU
	4.7 $\mu$ F X5R	0805	5	5	Near GPU
	330 $\mu$ F POS	7343	1	1	Near GPU ESR $\leq$ 6 m $\Omega$

### DA-07750-000-V02

Table 6. EDP-Continuous<sup>3</sup>

		GPU Core	GPU FBIO	FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>	1.35V Total <sup>2</sup>	3.3V Total <sup>2</sup>
		—	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.5V <sup>4</sup>	1.35V <sup>4</sup>	3.3V <sup>4</sup>
Products	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	19.0	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	2.4	2.3	0.80	0.06
N165-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80
	DDR3/L	26.0	1.4	2.4	2.3	0.80	0.06

Table 7. EDP-Peak<sup>3</sup>

		GPU Core	GPU FBIO	FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>	1.35V Total <sup>2</sup>	3.3V Total <sup>2</sup>
		—	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.5V <sup>4</sup>	1.35V <sup>4</sup>	3.3V <sup>4</sup>
Products	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	34.0	—	2.9	6.8	2.1	—
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N165-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1

### DA-07751-000-V02

Table 5. EDP-Continuous<sup>3</sup>

		GPU Core	GPU FBIO	FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>	1.35V Total <sup>2</sup>	3.3V Total <sup>2</sup>
		—	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.5V <sup>4</sup>	1.35V <sup>4</sup>	3.3V <sup>4</sup>
Product	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)
N165V-GMR1	GDDR5 @ 2.0 GHz	18.5	—	2.0	—	4.2	0.8
	GDDR5 @ 2.5 GHz	18.5	—	2.0	—	4.7	0.8
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8

Table 6. EDP-Peak<sup>3</sup>

		GPU Core	GPU FBIO	FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>	1.35V Total <sup>2</sup>	3.3V Total <sup>2</sup>
		—	1.5V <sup>4</sup>	1.35V <sup>4</sup>	1.5V <sup>4</sup>	1.35V <sup>4</sup>	3.3V <sup>4</sup>
Products	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)
N165V-GMR1	GDDR5 @ 2.0 GHz	30.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	31.0	—	3.1	—	7.2	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1

## VRAM GDDR5 chips

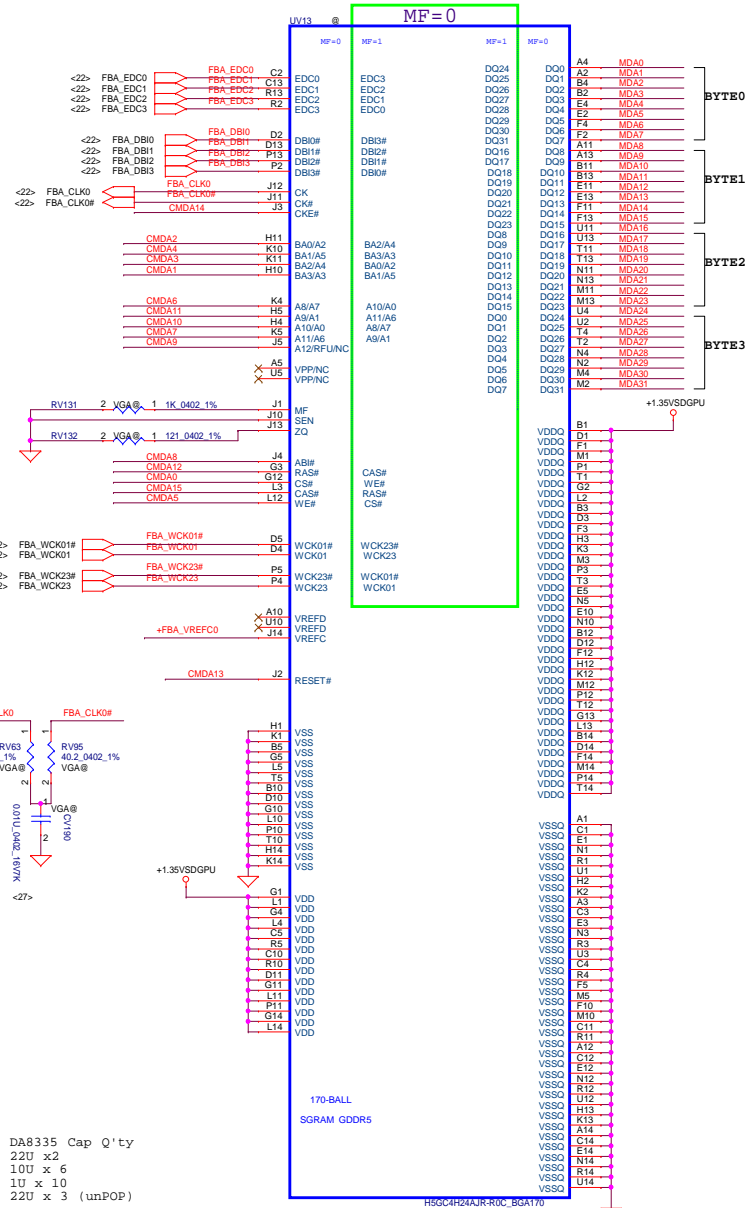


### X76 for N17S 2G VRAM

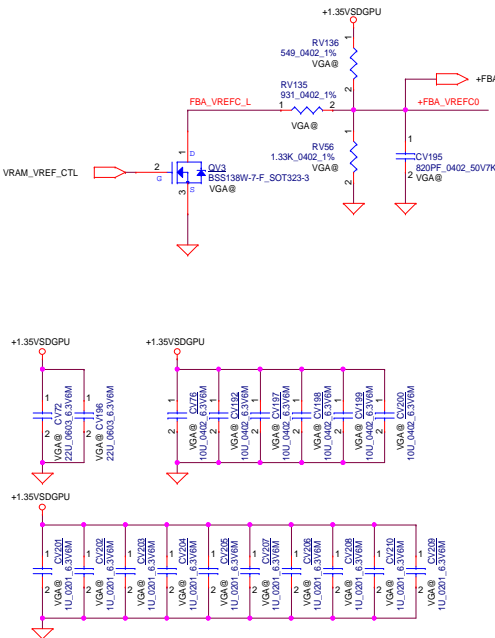


	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

### Channel 0 BOT SIDE



DA8335 Cap Q'ty  
22U x2  
10U x 6  
1U x 10  
22U x 3 (unPOP)

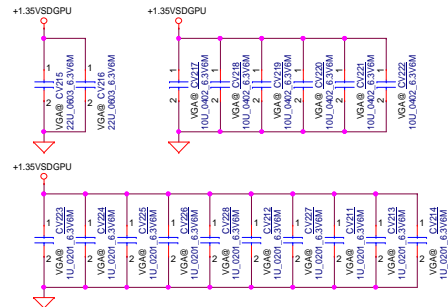


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	<b>N17S Lower Rank0 6/7</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Cost	<b>EH7LW M/B LA-H791P</b>
Date: Thursday, June 06, 2019				Sheet	26 of 57



## VRAM GDDR5 chips

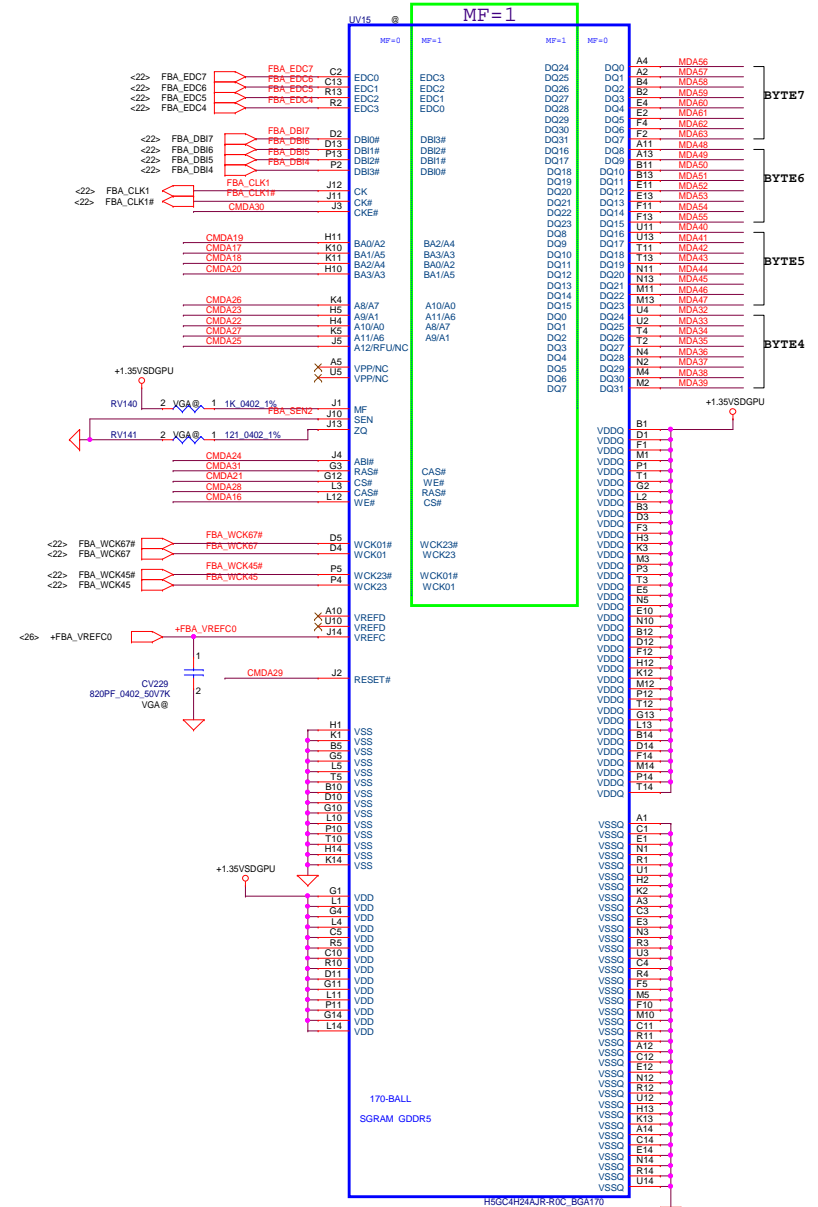
	DATA Bus	
Address	0...31	32...63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

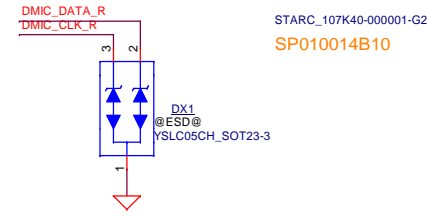
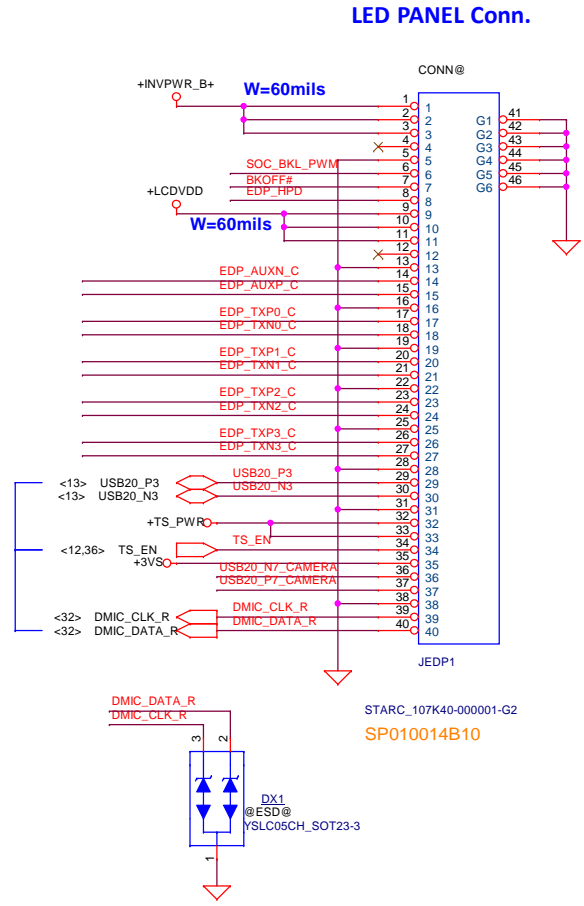
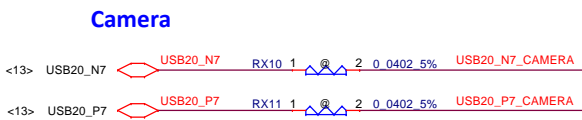
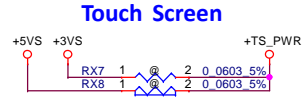
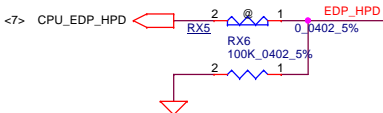
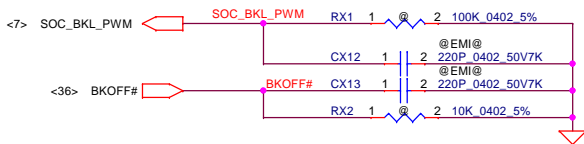
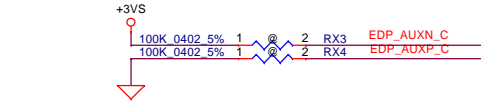
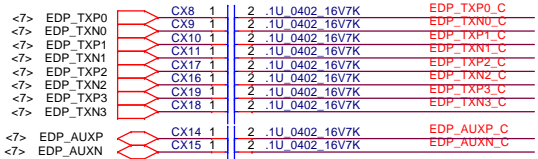
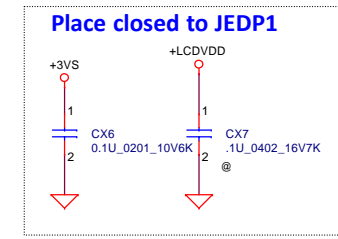
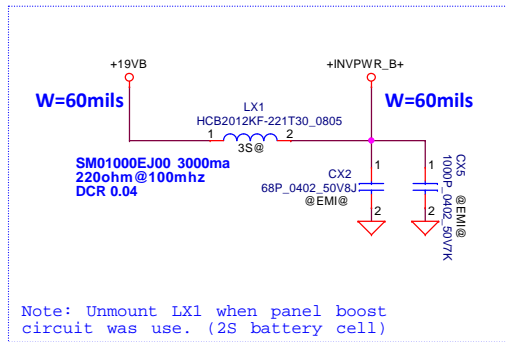
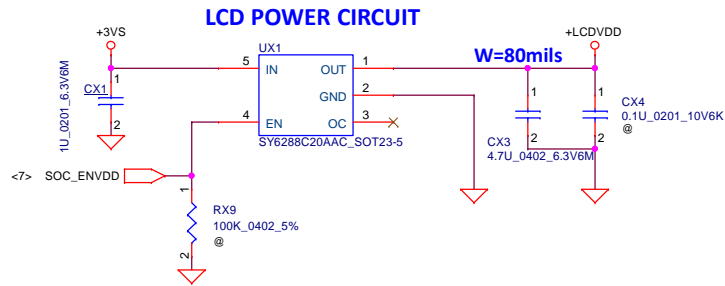


The diagram shows two signals, FBA\_CLK1 and FBA\_CLK1#. FBA\_CLK1 is a square wave with a period of 40.2 ns and a duty cycle of 40.2%. FBA\_CLK1# is an inverted square wave with the same period and duty cycle. A delay of 0.01 u is indicated between the two signals.

DA8335 Cap Q'ty  
22U x2  
10U x 6  
1U x 10  
22U x 3 (unPOP)

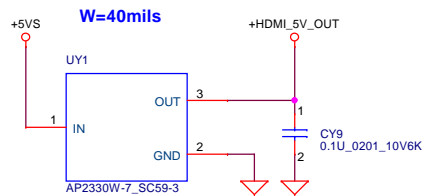
### Channel 1 BOT SIDE



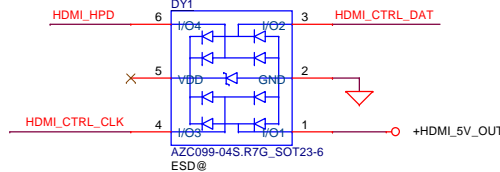
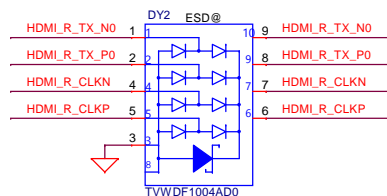
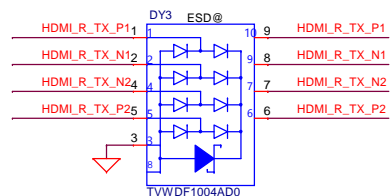
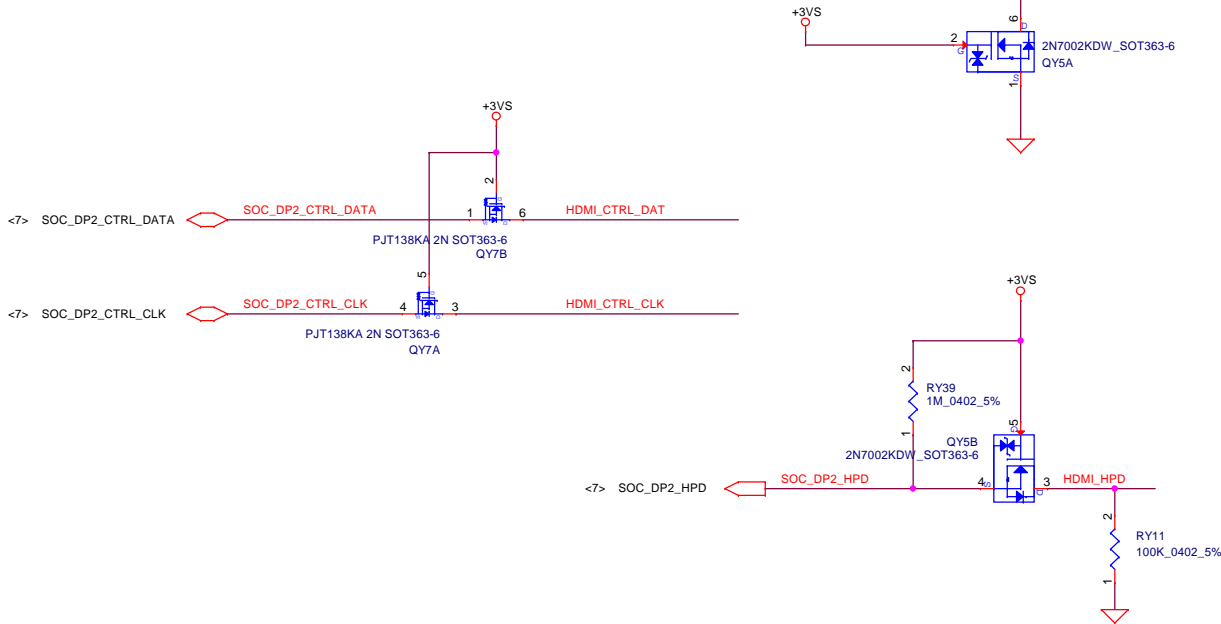
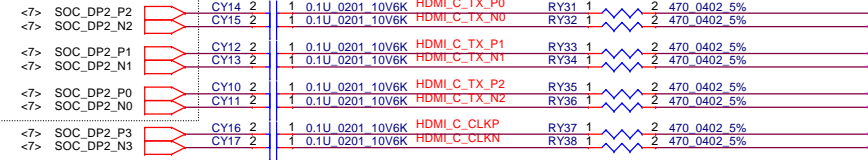


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				eDP Connector	
Size	Document Number	Rev		Date	
Custom	EH7LW M/B LA-H791P	0.2		Thursday, June 06, 2019	
Sheet		28		of	
Sheet		28		of	
Sheet		28		of	

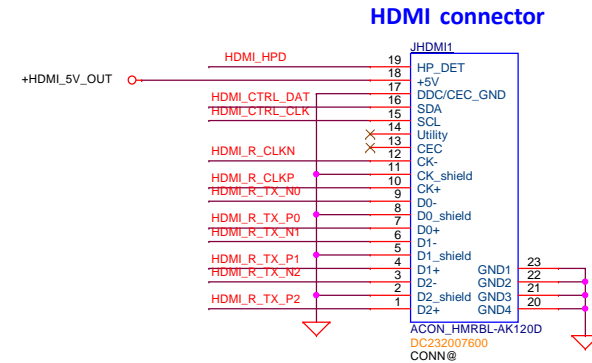
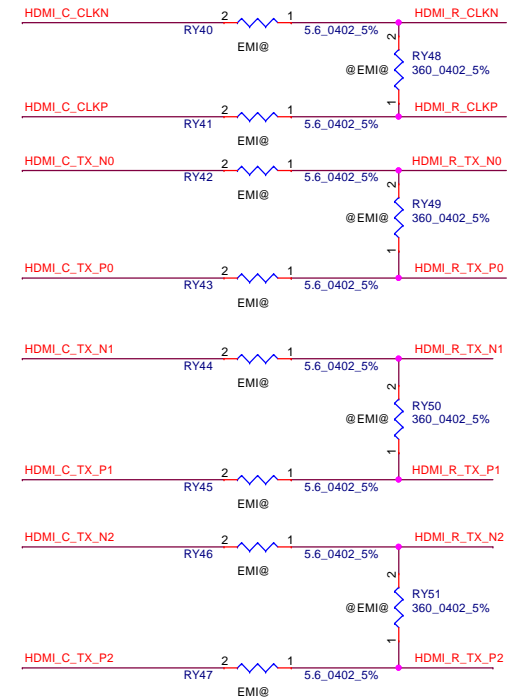
WWW.ALISALER.COM



port 0, 2 swap for INTEL HDMI



P/N: SC300001G00,S DIO(BR) AZC099-04S.R7G SOT23 ESD

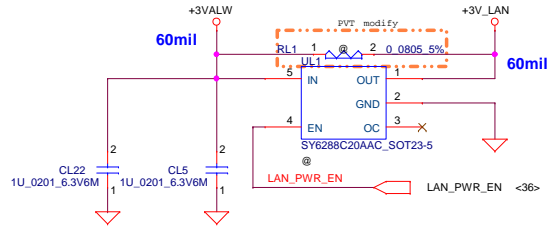


SYMBOL: DC232004700

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2018/12/27				Deciphered Date			
2018/12/27				2019/12/27				Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDMI CONN.				EH7LW M/B LA-H791P			
Date:				Thursday, June 06, 2019				Sheet			
				29				of			
				57				Rev			
				0.2							



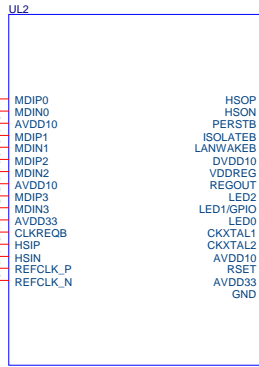
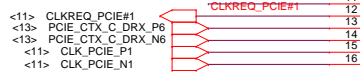
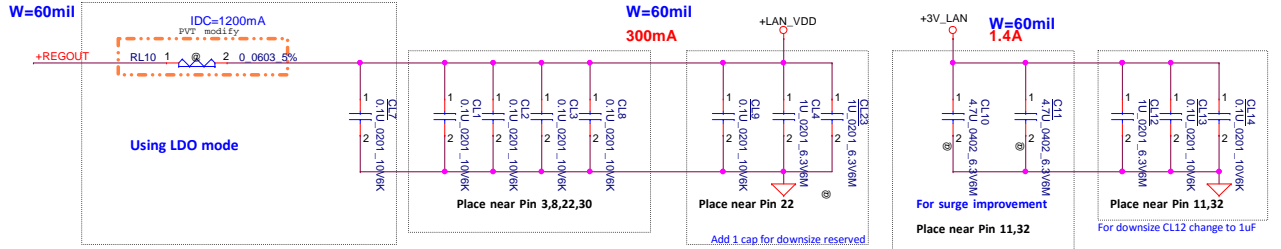
# LAN-RTL811H



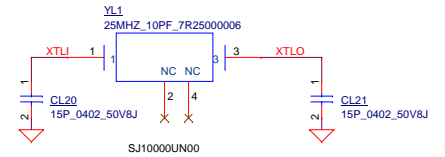
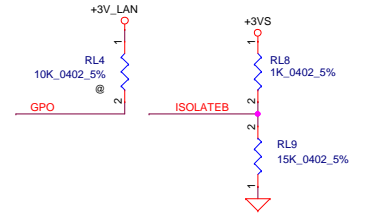
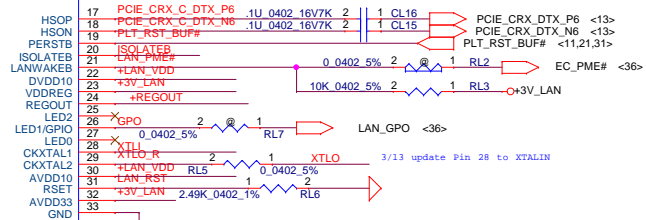
From EC

High active  
EN threshold voltage min:1.2V typ:1.6V max:2.0V  
Current limit threshold 1.5~2.8A

+3V\_LAN Rising time must >0.5 ns and <100 ns

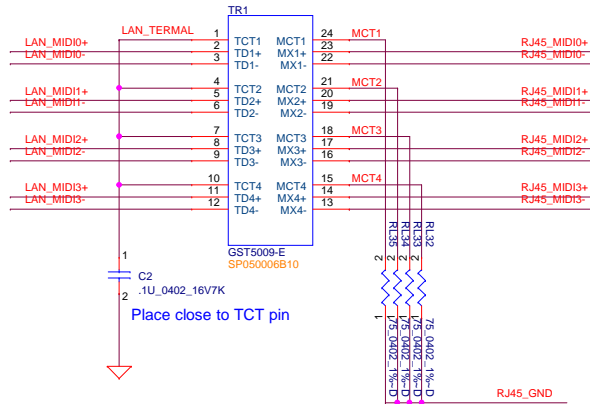
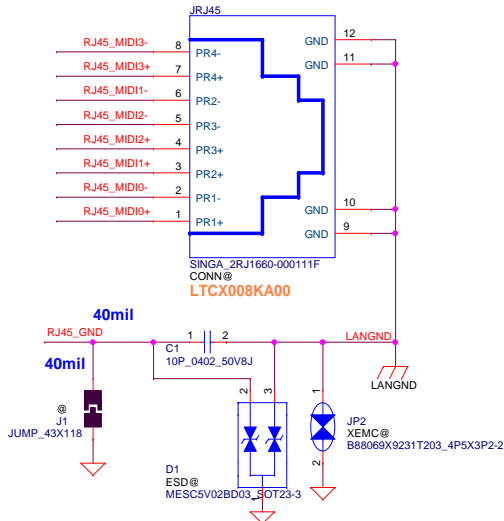


RTL8111H-CG\_QFN32\_4X4  
SA000080P00



12/21 change YL1 size to 20x16

## LAN Connector



Security Classification		Compal Secret Data	
Issued Date	2018/12/27	Deciphered Date	2019/12/27
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>			

**Compal Electronics, Inc.**

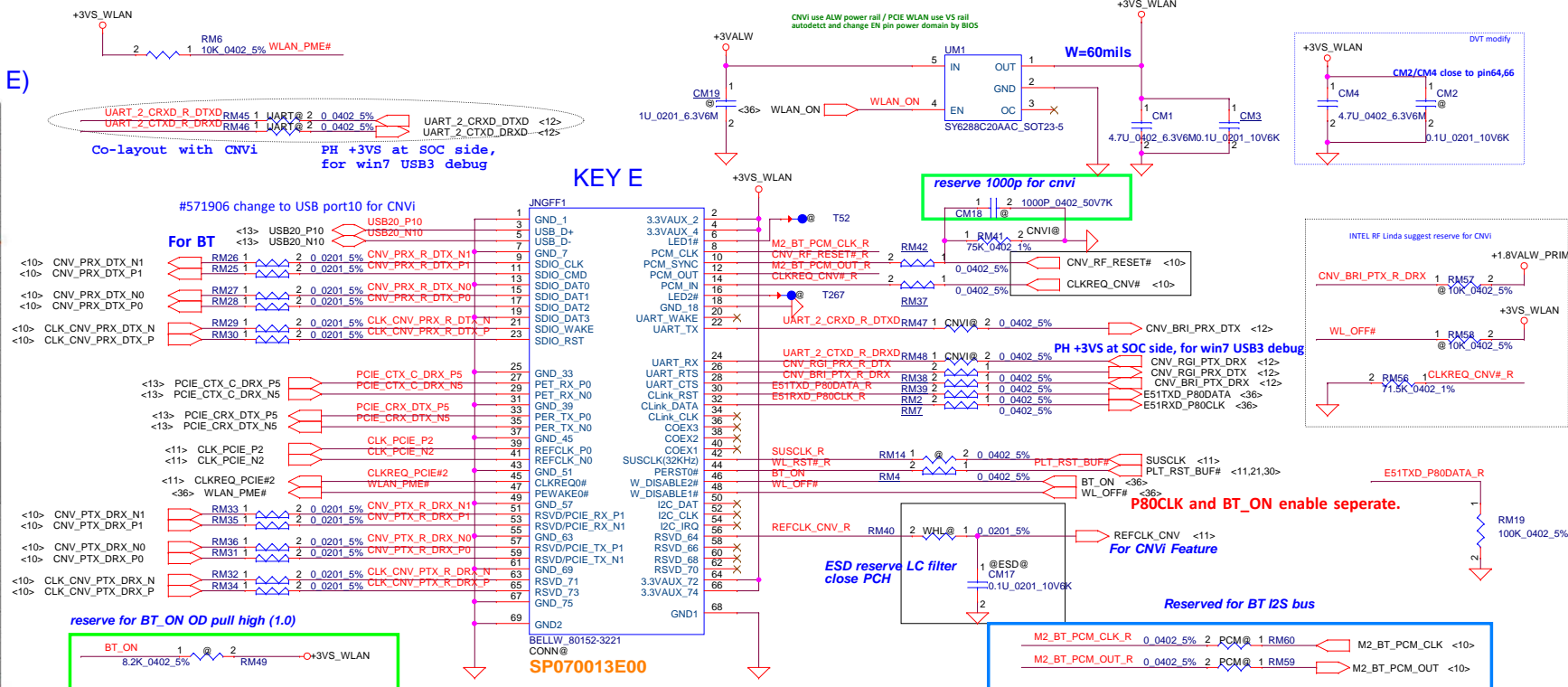
**LAN RTL8111H-CG**

Size	Document Number
Custom	<b>EH7LW M/B LA-H791P</b>

WWW.ALISALER.COM

## Wireless LAN

## NGFF WL+BT (KEY E)

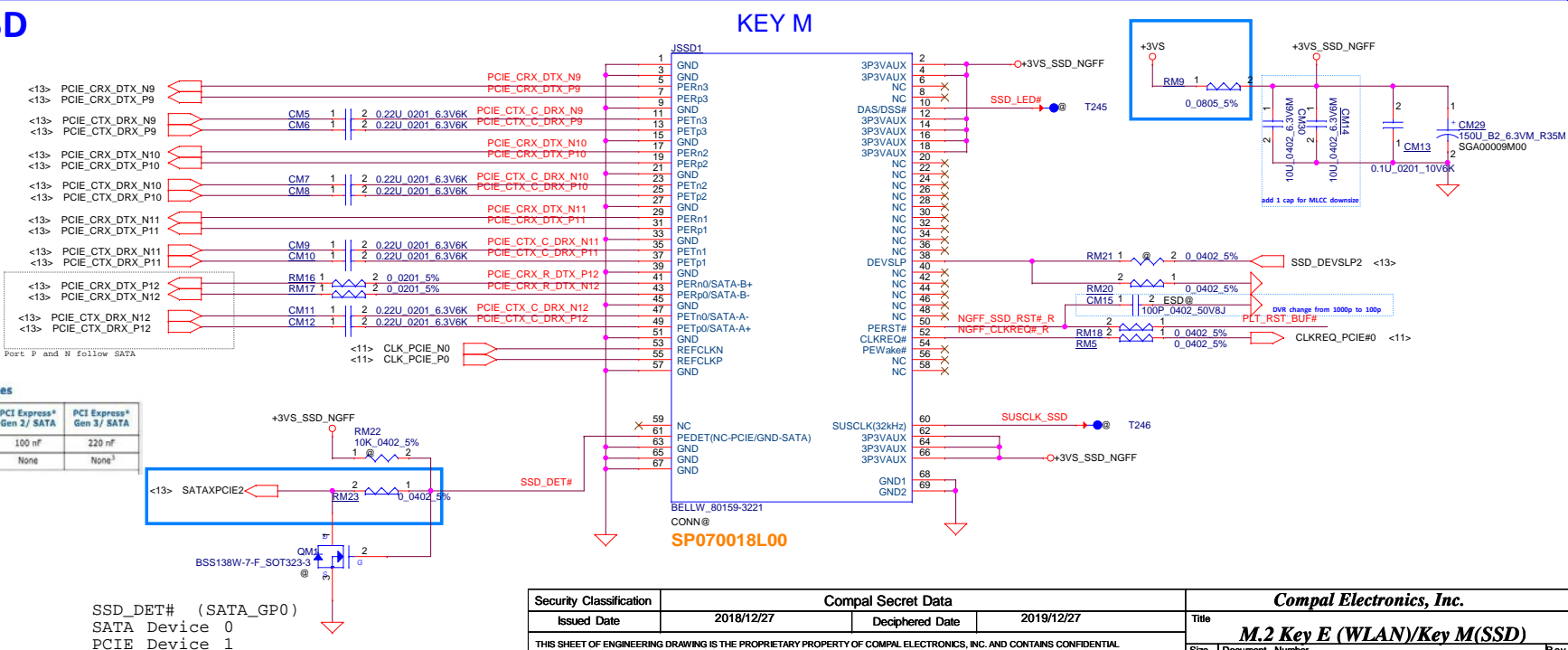


## mSATA/SSD

PETp0/SATA-A+	49
PETn0/SATA-A-	47
GND	45
PERp0/SATA-B-	43
PERn0/SATA-B+	41

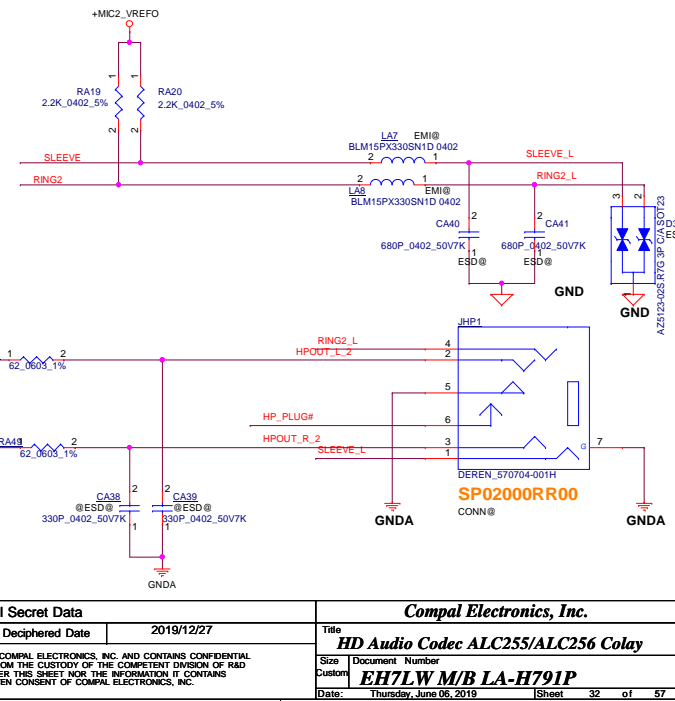
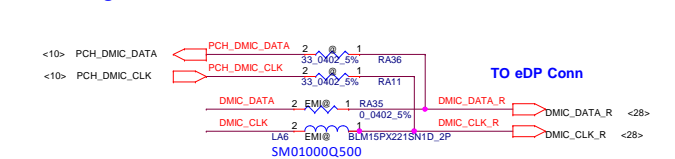
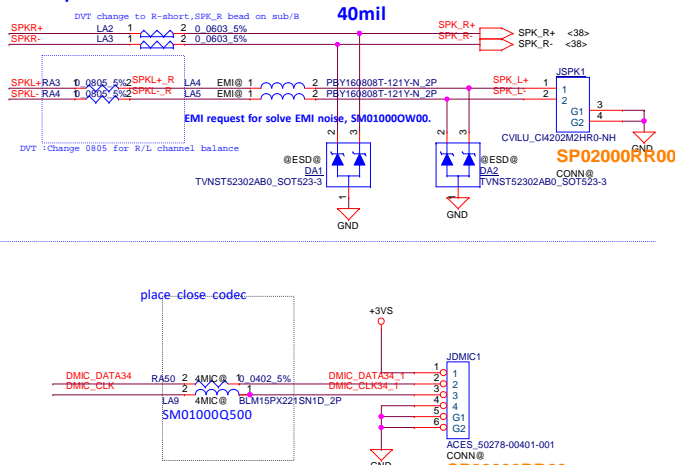
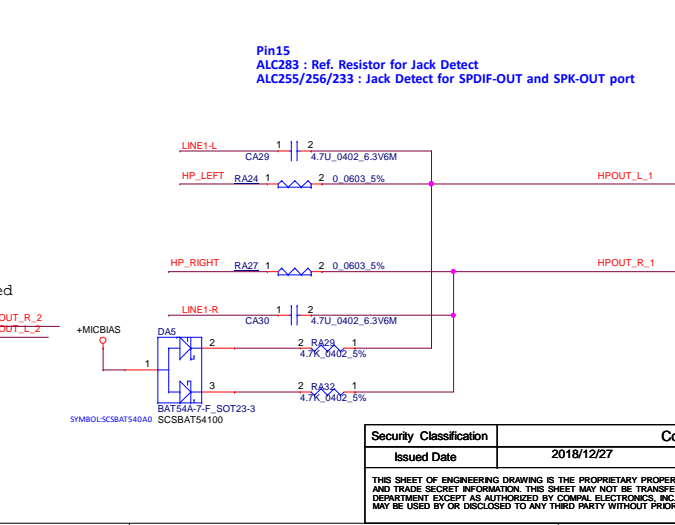
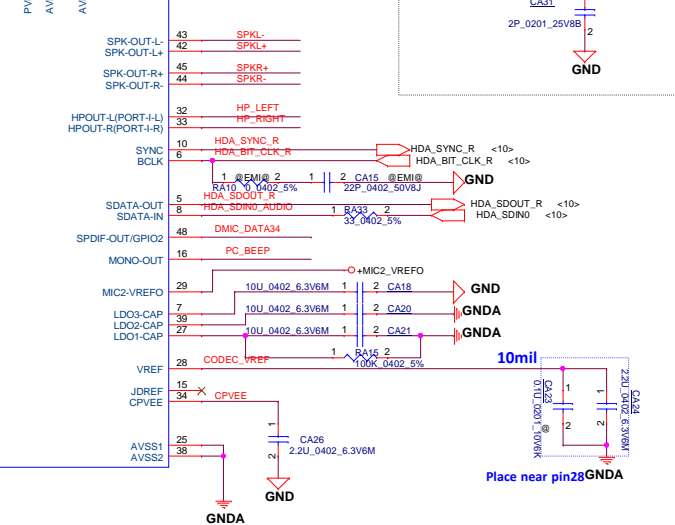
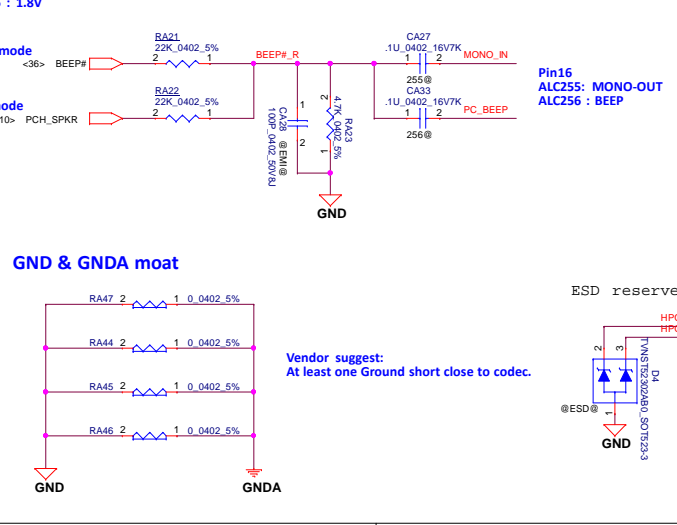
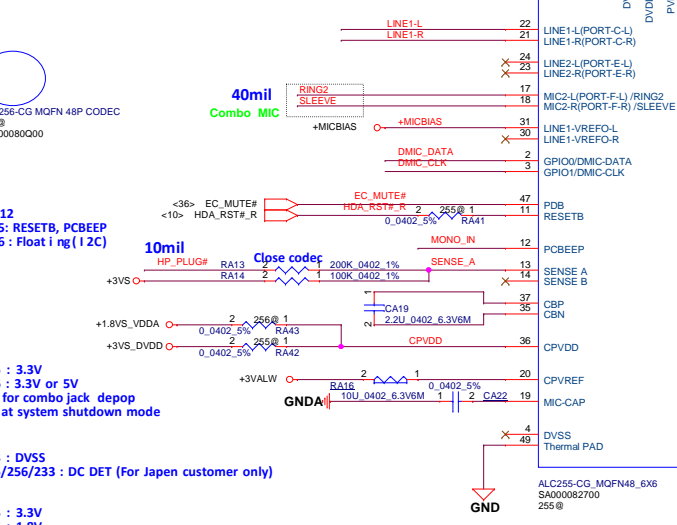
Table 35-7. SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>



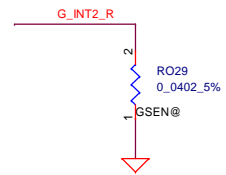
```
SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1
```

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>			
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>M.2 Key E (WLAN)/Key M(SSD)</b>			
				Size	Document Number	Rev	
				Cust	<b>EH7LW M/B LA-H791P</b>	0.2	
Date:		Thursday, June 06, 2019		Sheet	31	of	57

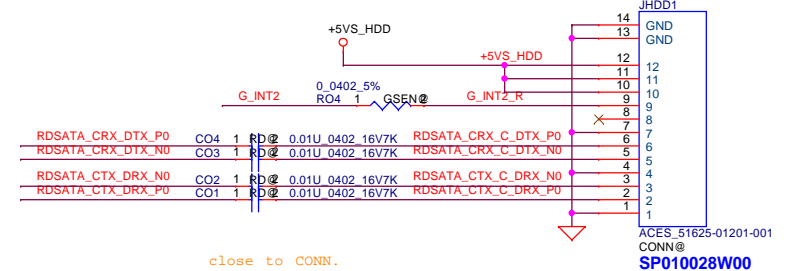


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	HD Audio Codec ALC255/ALC256 Colay
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custian	EH7LW M/B LA-H791P
				Date:	Thursday, June 06, 2019
				Sheet	32 of 57

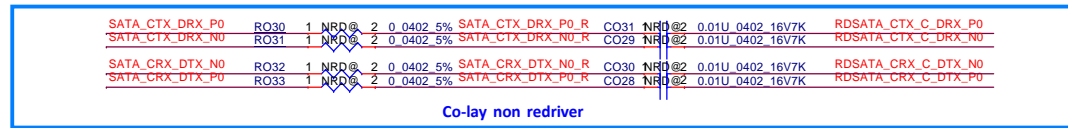
[WWW.ALISALER.COM](http://WWW.ALISALER.COM)



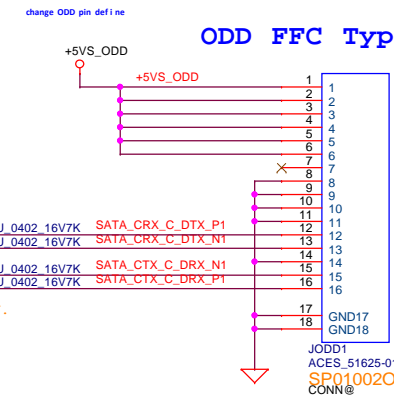
HDD	FFC	Type
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
18	18	18
19	19	19
20	20	20
21	21	21
22	22	22
23	23	23
24	24	24
25	25	25
26	26	26
27	27	27
28	28	28
29	29	29
30	30	30
31	31	31
32	32	32
33	33	33
34	34	34
35	35	35
36	36	36
37	37	37
38	38	38
39	39	39
40	40	40
41	41	41
42	42	42
43	43	43
44	44	44
45	45	45
46	46	46
47	47	47
48	48	48
49	49	49
50	50	50
51	51	51
52	52	52
53	53	53
54	54	54
55	55	55
56	56	56
57	57	57
58	58	58
59	59	59
60	60	60
61	61	61
62	62	62
63	63	63
64	64	64
65	65	65
66	66	66
67	67	67
68	68	68
69	69	69
70	70	70
71	71	71
72	72	72
73	73	73
74	74	74
75	75	75
76	76	76
77	77	77
78	78	78
79	79	79
80	80	80
81	81	81
82	82	82
83	83	83
84	84	84
85	85	85
86	86	86
87	87	87
88	88	88
89	89	89
90	90	90
91	91	91
92	92	92
93	93	93
94	94	94
95	95	95
96	96	96
97	97	97
98	98	98
99	99	99
100	100	100



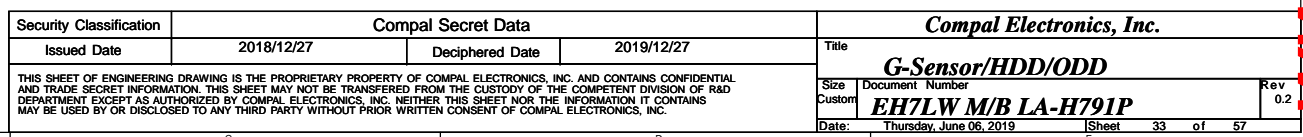
CONN@  
SP010028W00



ODD FFC Type

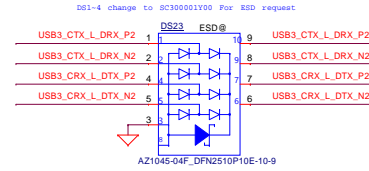
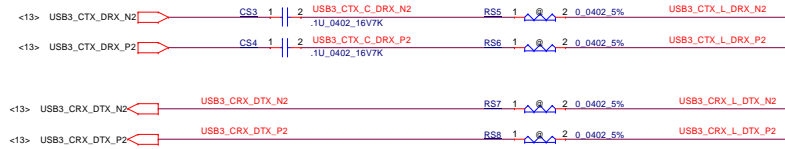


ACES\_51625-01601-001  
SP01002OK00  
CONN@

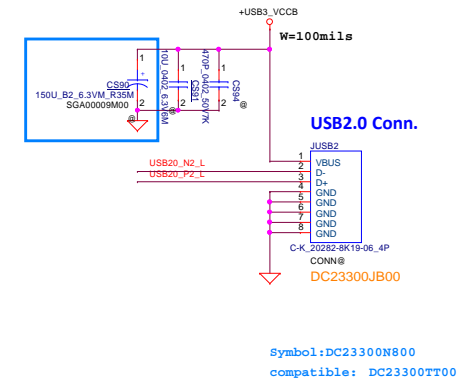
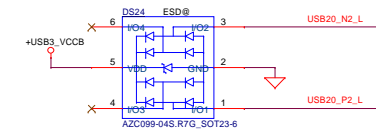
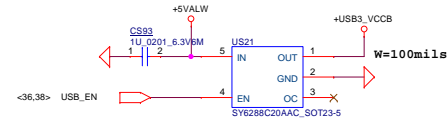
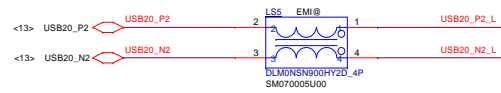


## USB3.0 (Port 2)

USB3 port reserved

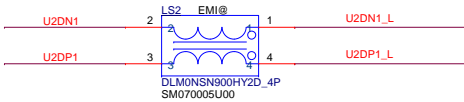
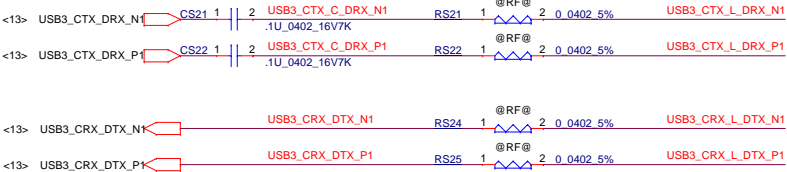


## USB2.0 (Port 2)

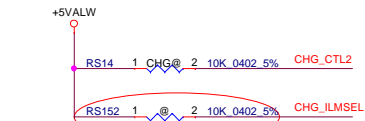
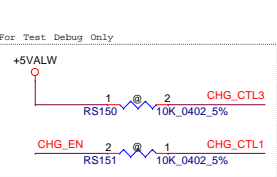
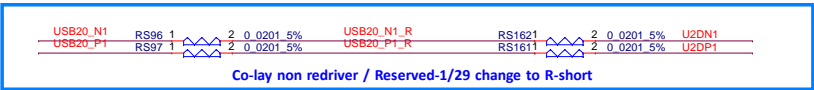


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2018/12/27	Title	USB3 P2 MB
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	EH7LW M/B LA-H791P
				Date:	Thursday, June 06, 2019
				Sheet	34 of 1

USB3.0 (Port 1)



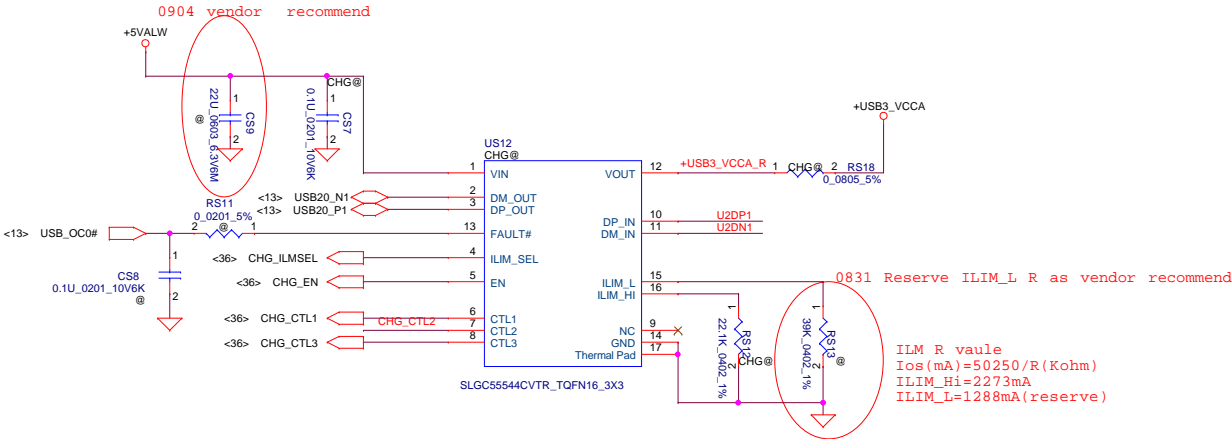
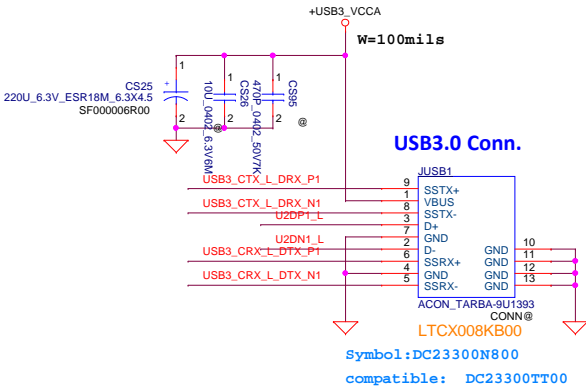
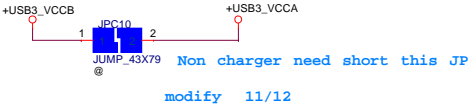
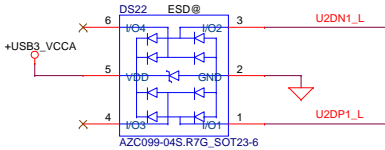
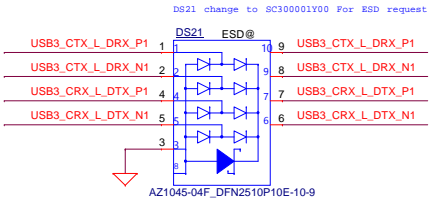
DVT: R-short



Reserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB3 P1 CHG MB
Size	Document Number	Rev	Date: Thursday, June 06, 2019   Sheet 35 of 57	
Custom	EH7LW M/B LA-H791P	0.2		

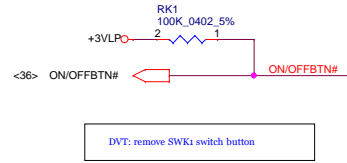




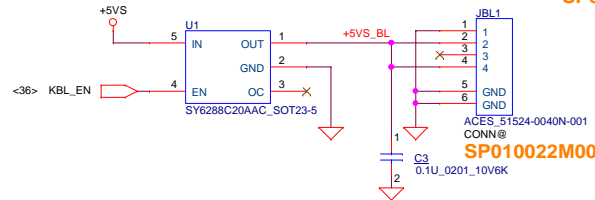


## KB Conn.

### ON/OFF BTN



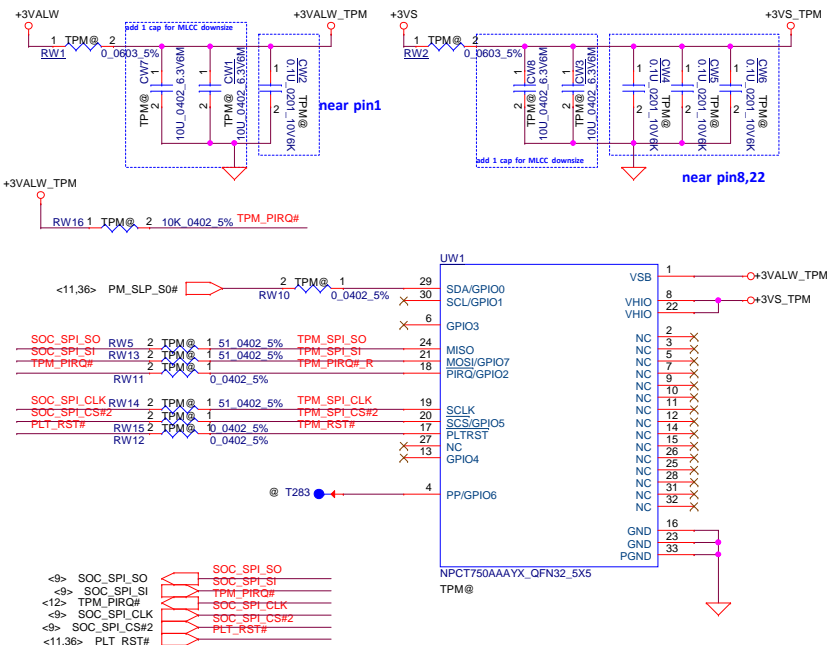
## KB BackLight



SP01000GO00

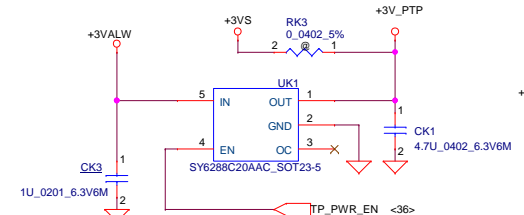
SP010022M00

## TPM 2.0

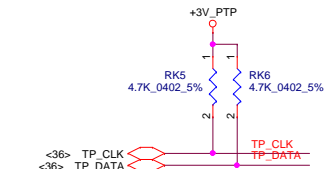
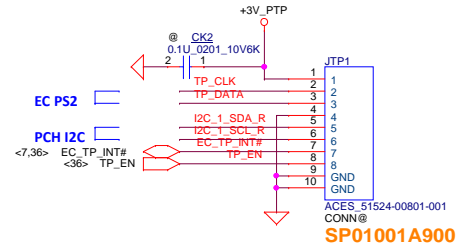
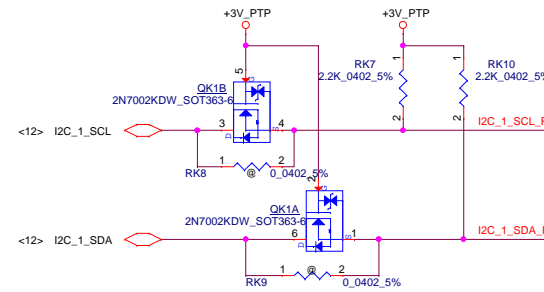


SA0000AQ230, 5 IC NPCT750AAAYX QFN 32P TPM (SPI interface)

## TP/B Conn.

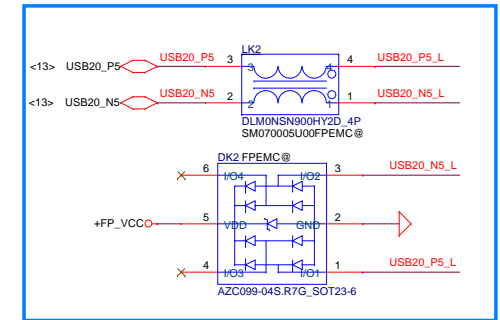
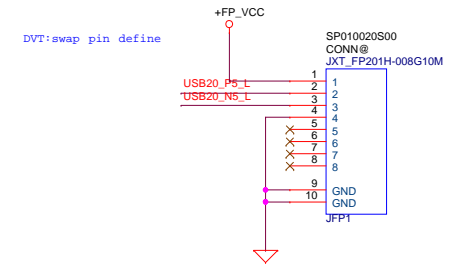
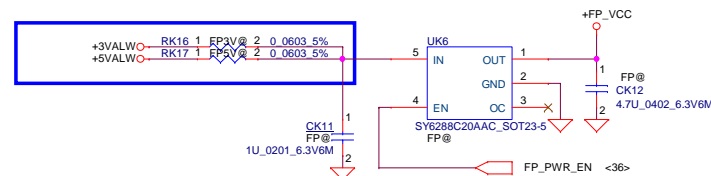


TP\_PWR\_EN follow SYSON behavior



## Finger Print

Power Souce Check  
EGIS ETU801 +FP\_VCC=5V  
ELAN SA464K-2200 +FP\_VCC=3.3V



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2018/12/27		Deciphered Date		2019/12/27		Title			
								KB & TP & TPM & FP			
Size		Document Number		Customer		Rev		EH7LW M/B LA-H791P			
Date:		Thursday, June 06, 2019		Sheet		37		of 57			

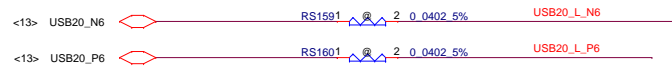
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

## USB I/O



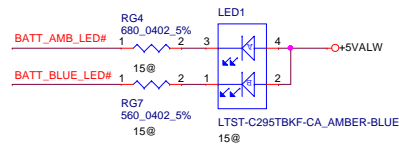
Reserved CMC on SUB/B side

## Card reader

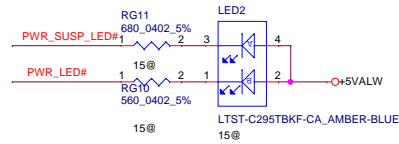


## LED for 15" UMA

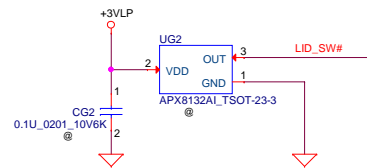
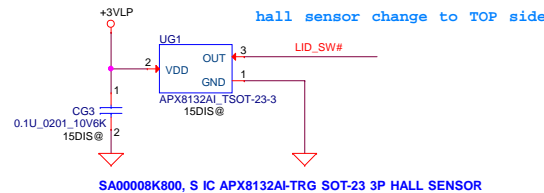
### Battery LED



### Power LED

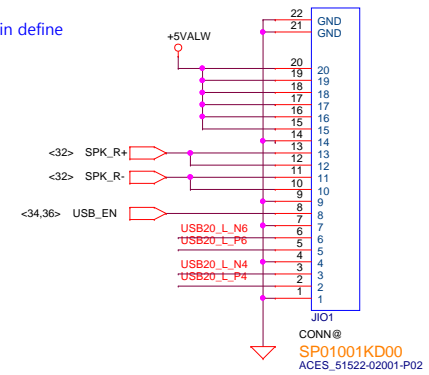


## LID for 15" DIS

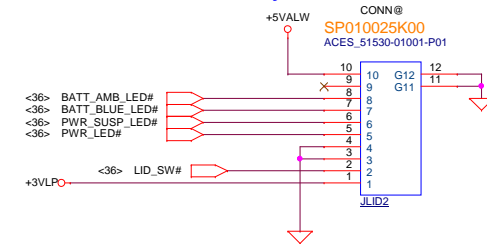


## I/O Borad (USB2 /Card reader/ Speaker-RCH)

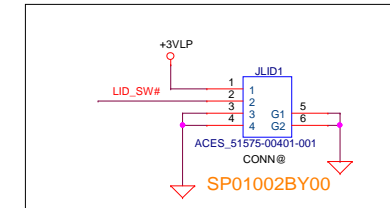
DVT:update JIO1 pin define



## LID/B with LED for 17" UMA & DIS

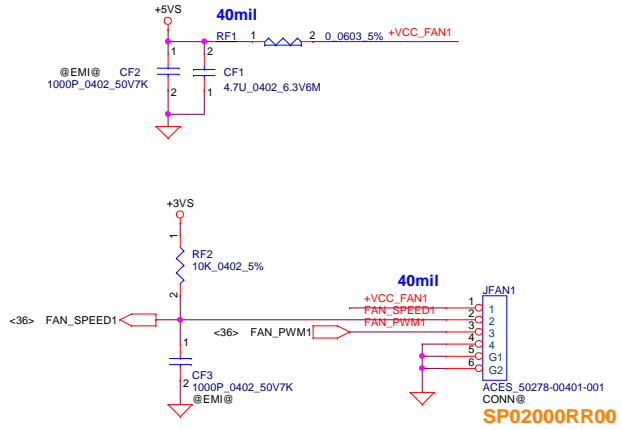


## LID/B for 15" UMA 4pin

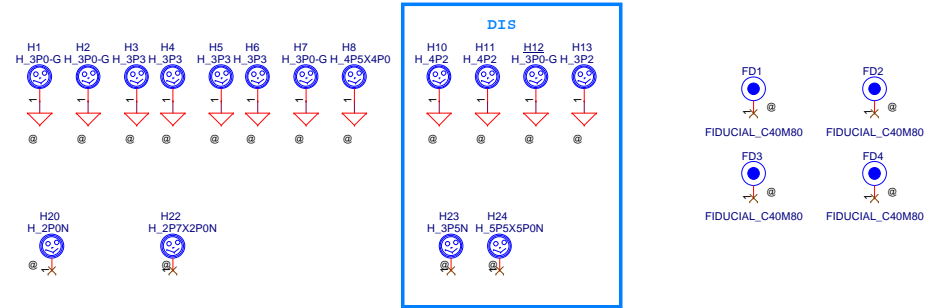


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2018/12/27		Deciphered Date		2019/12/27	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		IO/LiD/LED	
				Size		Document Number	
				EH7LW M/B LA-H791P		0.2	
				Date:		Thursday, June 06, 2019	
				Sheet		38 of 57	

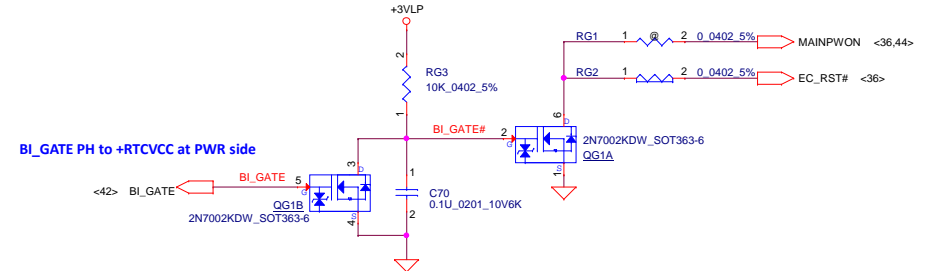
## FAN1 Conn



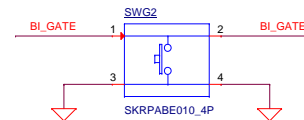
## Screw Hole



## Reset Circuit

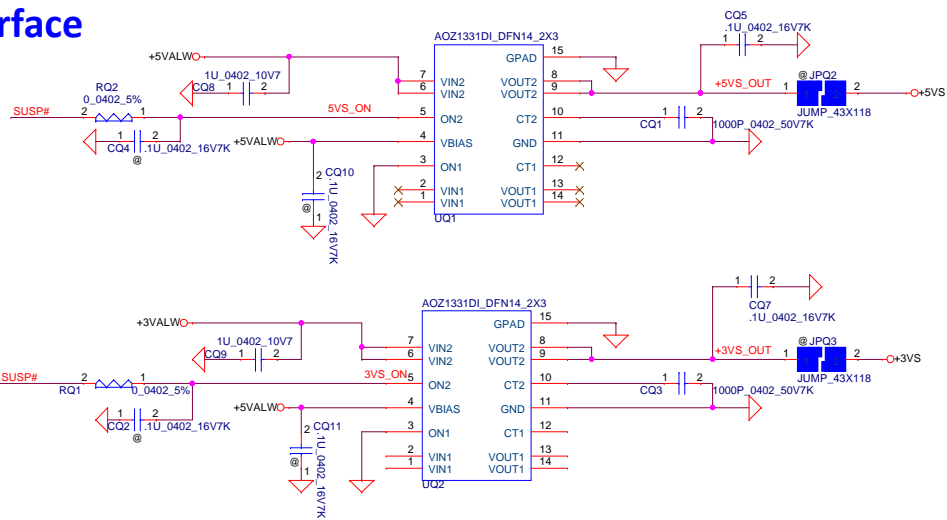


## Reset Button

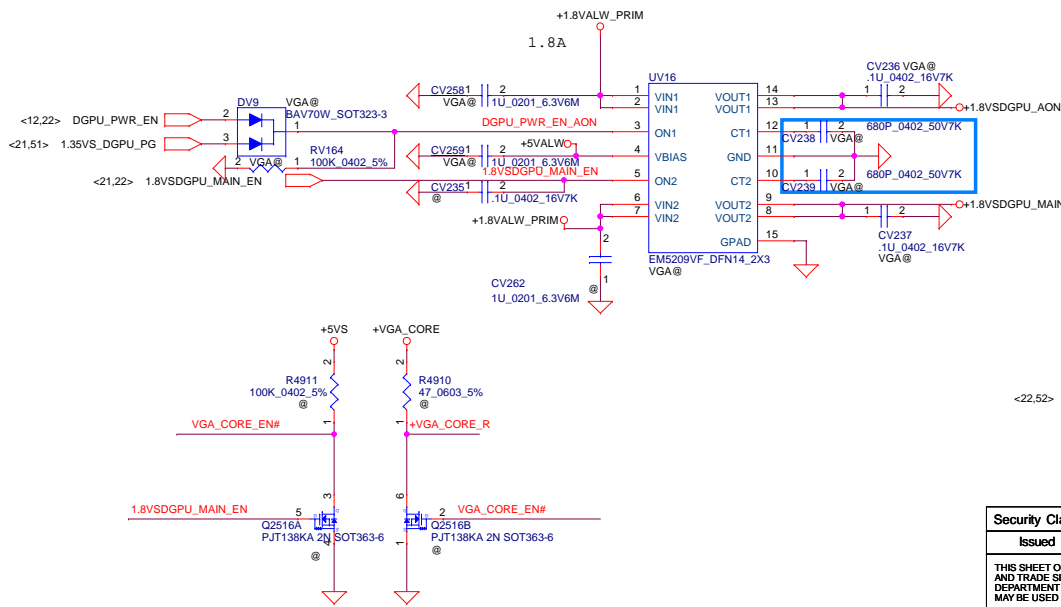
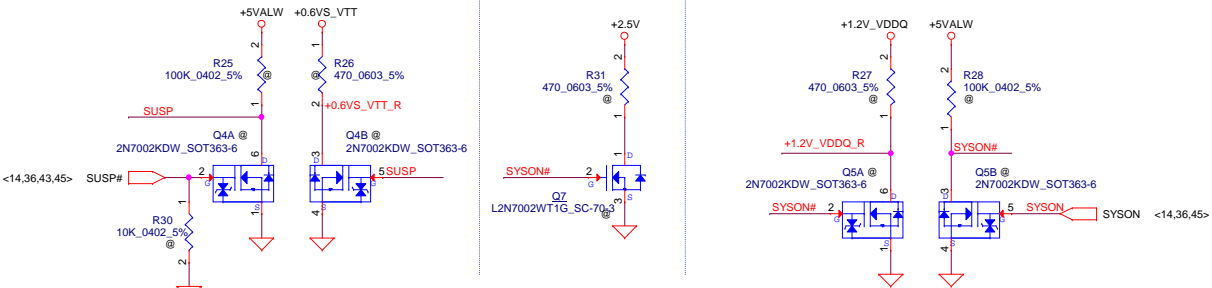
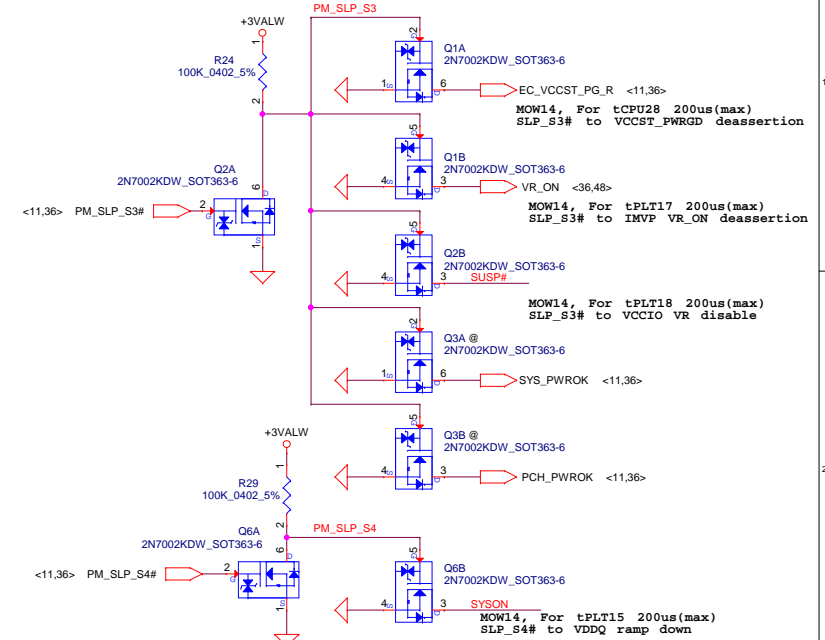


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>FAN &amp; Screw Hole &amp; Reset</b> Title	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 0.2	EH7LW M/B LA-H791P Date: Thursday, June 06, 2019
				Sheet 39 of 57	

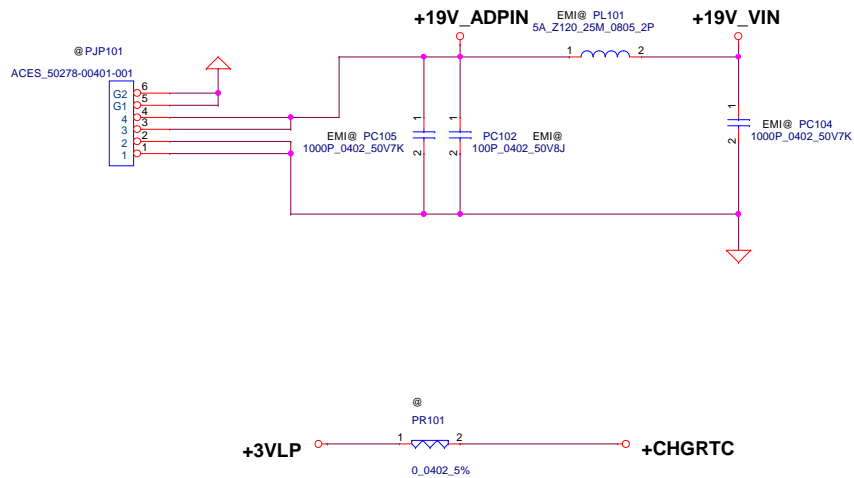
## DC Interface



## For Power ON/Off Sequence



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				DC Interface	
				Size	Document Number
				Customer	EH7LW M/B LA-H791P
				Date	Thursday, June 06, 2019
				Sheet	40 of 57

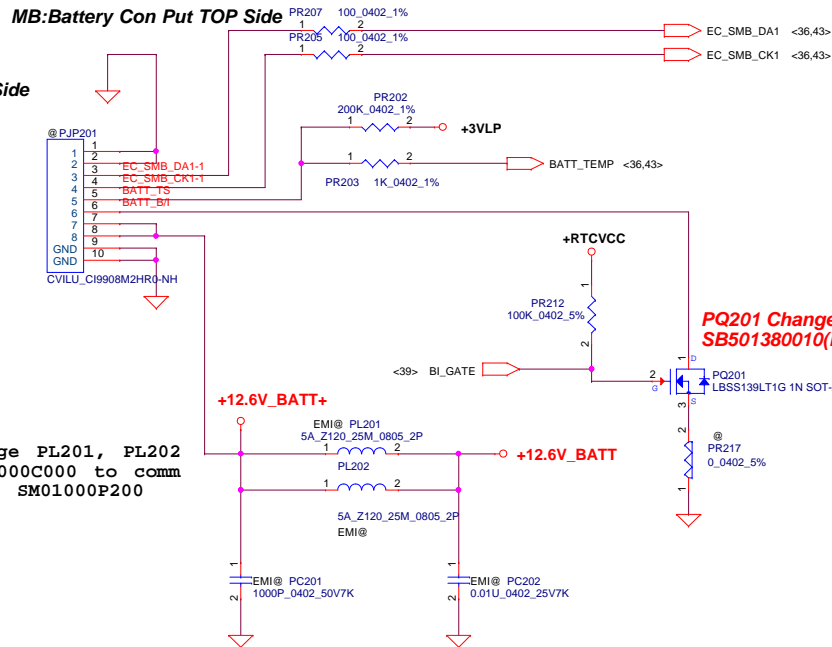


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/12/27	Deciphered Date	2019/12/27	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Document Number	Rev
		Custom		EH7LW M/B LA-H791P	0.2
		Date:		Thursday, June 06, 2019	Sheet 41 of 57



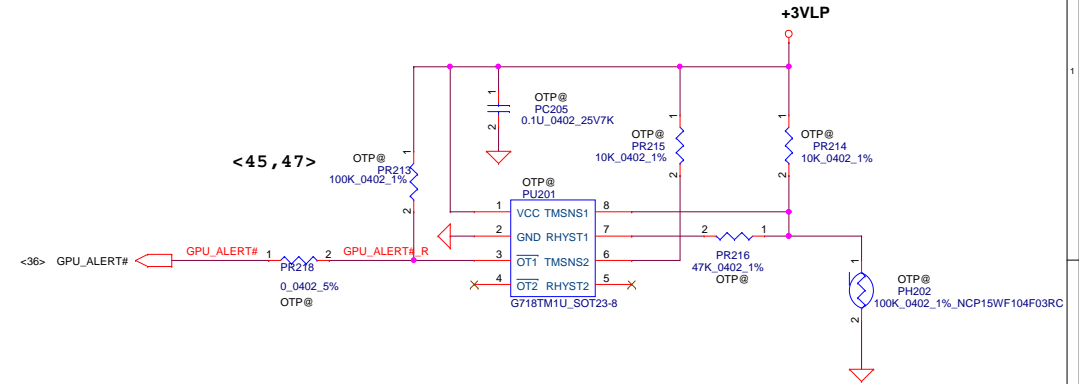
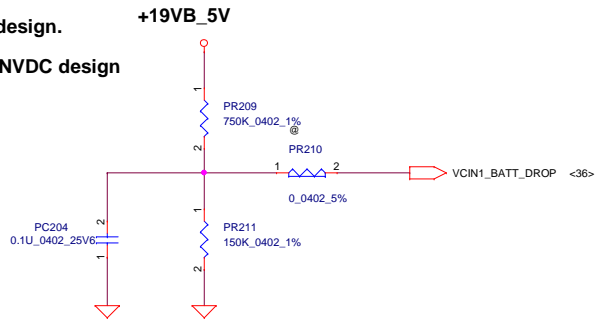
## Battery Bot Side

PIN1 GND  
PIN2 GND  
PIN3 SMD  
PIN4 SMC  
PIN5 TEMP  
PIN6 BI  
PIN7 Batt+  
PIN8 Batt+



**2013/06/07**  
**Add for ENE9022 Battery Voltage drop detection.**  
**Connect to ENE9022 pin64 AD1.**

**VAL50/ZAL20 Battery is 3-cell NVDC design.**  
**B+=9V**  
**Change PR12=50K if Battery is 2-cell NVDC design**  
**B+=6V**

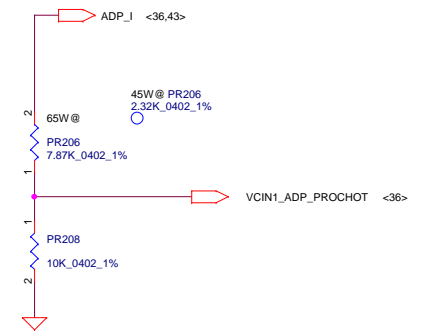
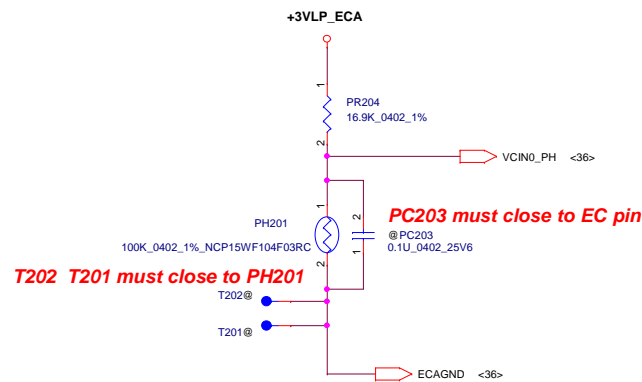


**PQ201 Change to SB00000Q000,  
SB501380010(BSS138LT1G Del)**

**2016/11/16 update**

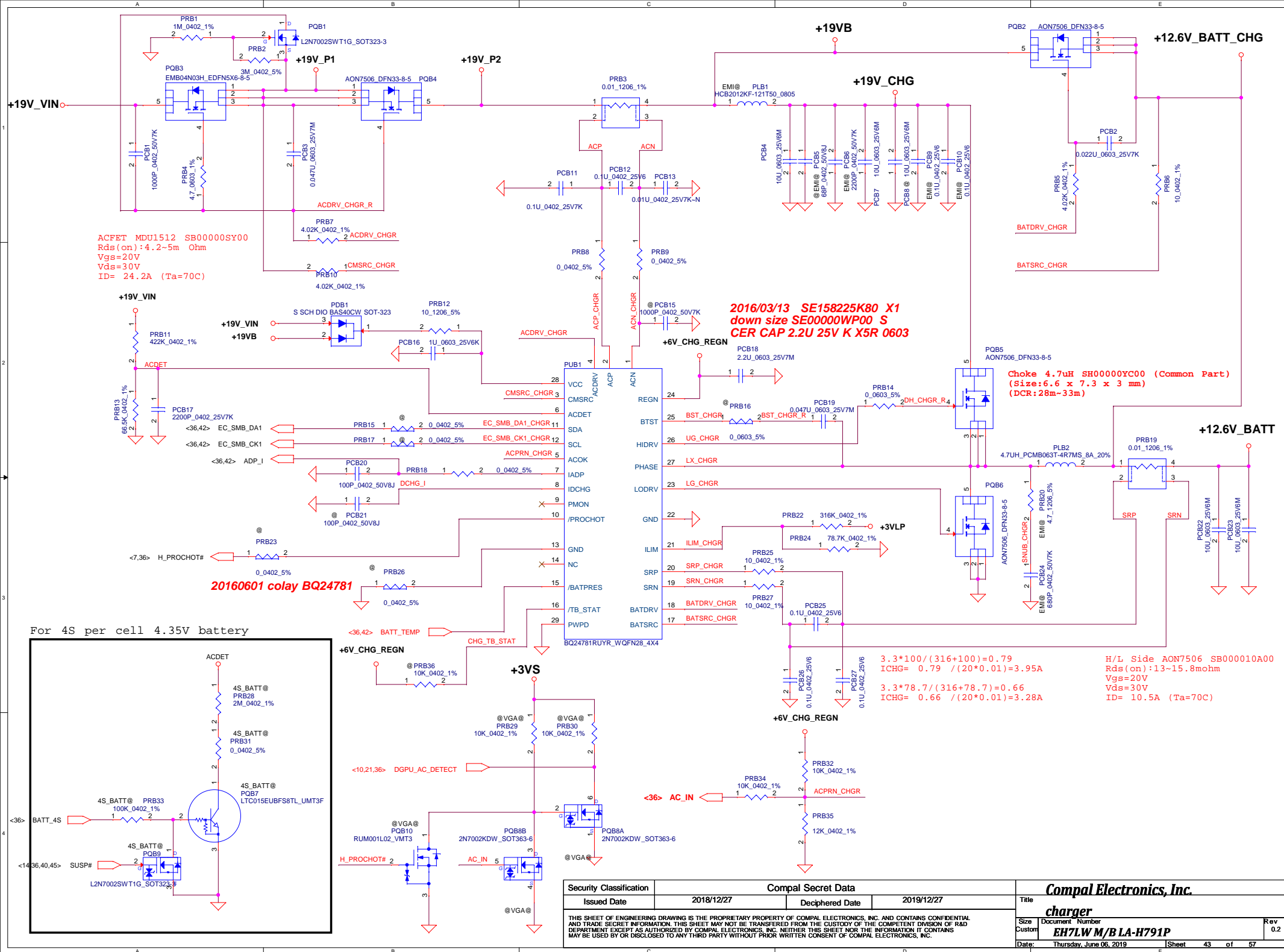
For KB9022 sense 20mΩ	Active	Recovery
45W PR206 2.32K ohm	58.5W, 1V	Active=recovery
65W PR206 7.87K ohm	84.5W, 1V	Active=recovery
90W PR20K ohm	__W, __V	Active=recovery
PH1	2V	1V

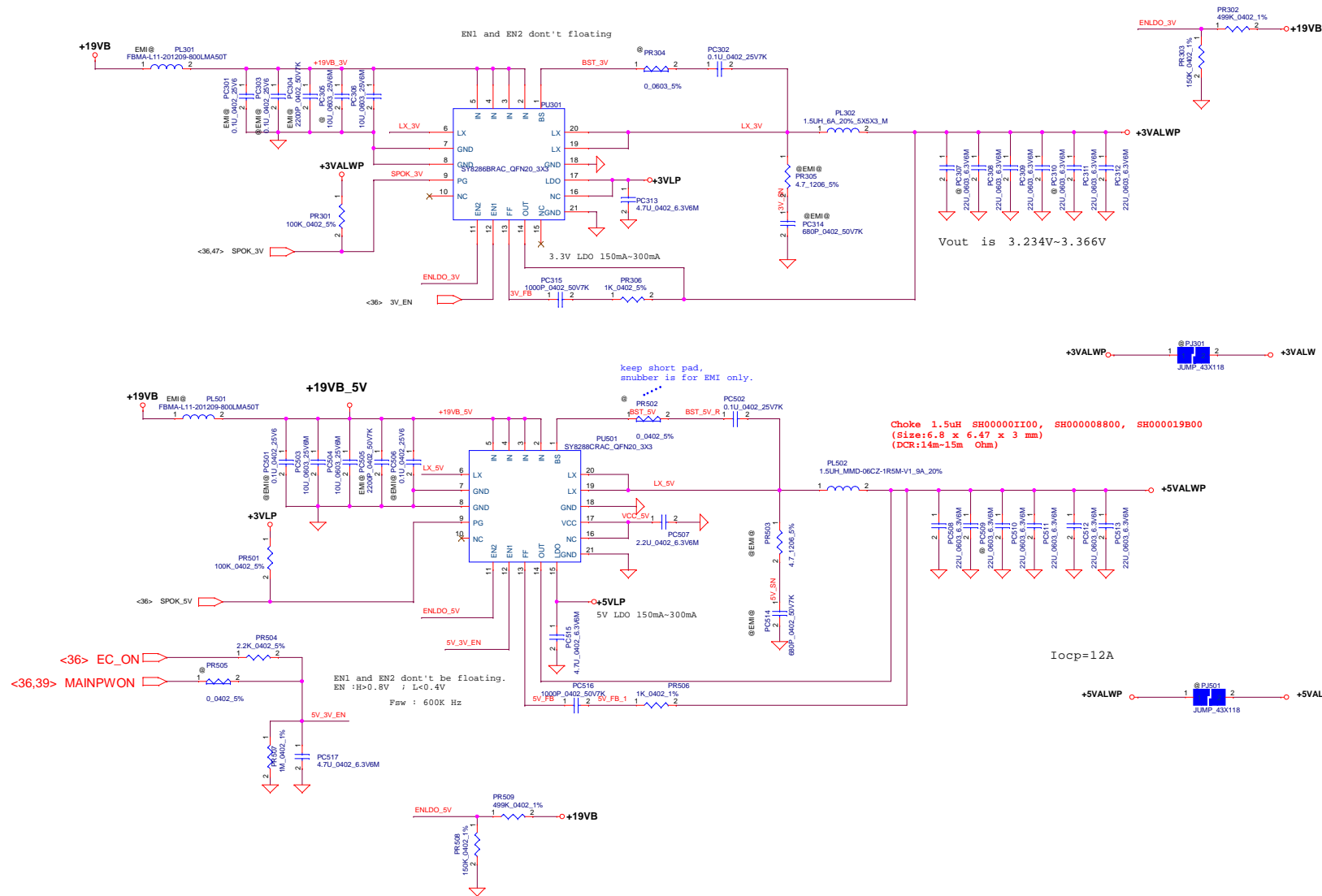
**PH1 under CPU botten side :**  
**CPU thermal protection at 89 +-3 degree C**  
**Recovery at 56 +-3 degree C**



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2018/12/27	Deciphered Date		2019/12/27	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		
				PWR-BATTERY CONN/OTP		
Size		Document Number			Rev	
Custom		EH7LW M/B LA-H791P			0.2	
Date:		Thursday, June 06, 2019		Sheet	42 of 57	

**WWW.ALISALER.COM**

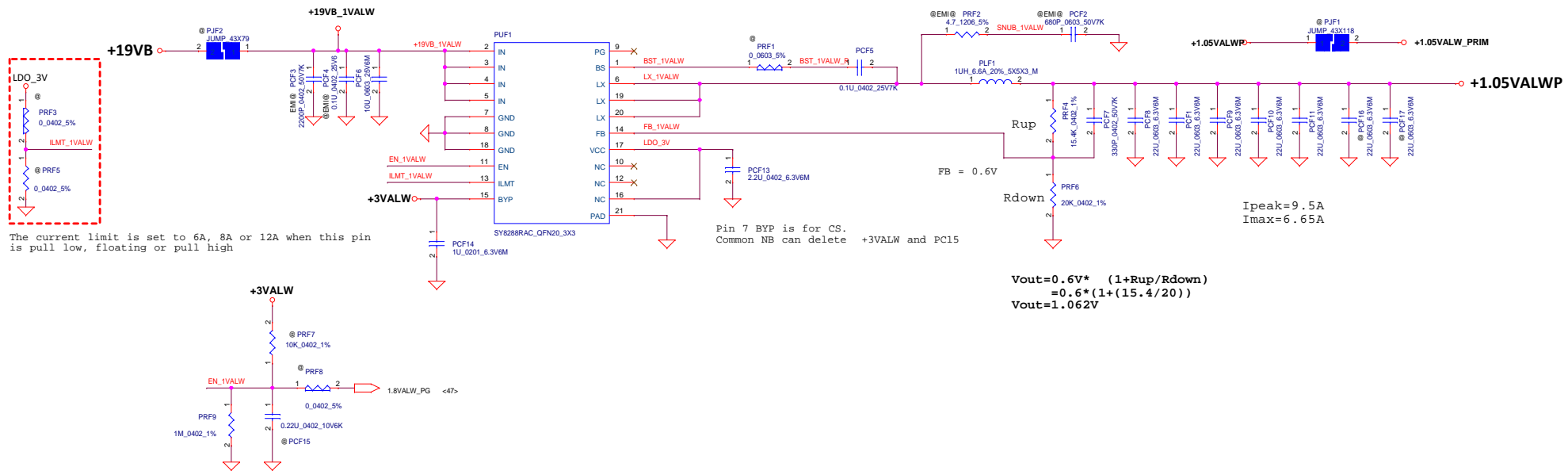




Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	+3VALW/+5VALW
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number	Rev
				Custom	0.2
				Date: Thursday, June 06, 2019	Sheet 44 of 57

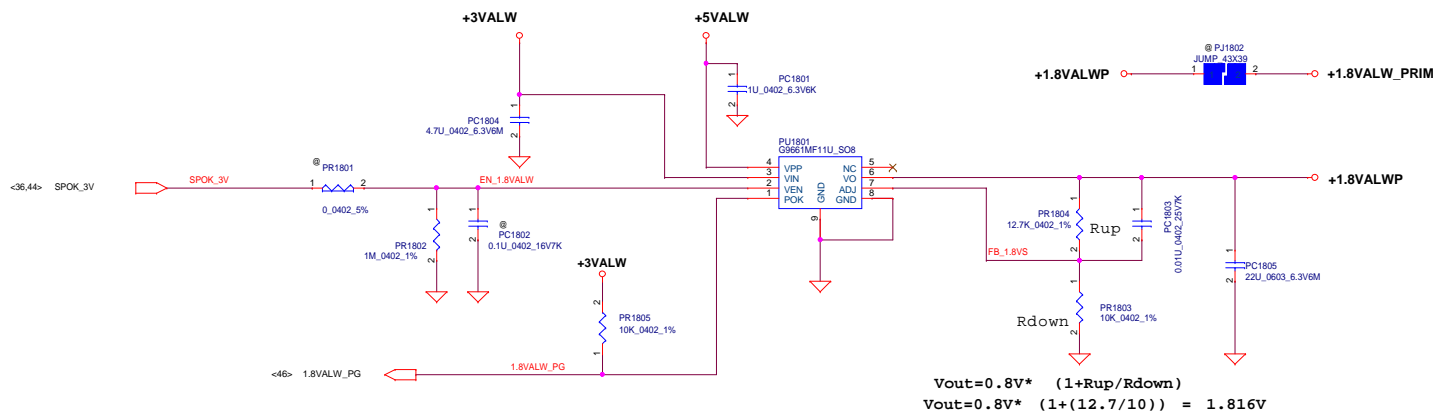


EN pin don't floating  
If have pull down resistor at HW side, pls delete PR702

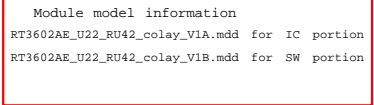


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	VCCP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				C	EH7LW M/B LA-H791P
				Date:	Thursday, June 06, 2019
				Sheet	46 of 57
				Rev	0.2





Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	SY8032
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				C	EH7LW M/B LA-H791P
				Date:	Thursday, June 06, 2019
				Sheet	47 of 57
				Rev	0.2



PRZ59 and PRZ60 are for debug only.  
VCCGT\_SENSE and VSSGT\_SENSE need other resistor  
at HW side.



2017/07/03  
VCORE Output Capacitor:  
U42  
22uF\_0603\*35  
1uF\_0201\*35  
220uF \*2  
UNPOP  
22uF\_0603\*35  
220uF \*2

2017/07/03  
VCORE Output Capacitor:  
U22  
22uF\_0603\*29  
1uF\_0201\*35  
UNPOP  
22uF\_0603\*35  
220uF \*2

WWW.ALISALER.COM

SGA2020221D4 0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/12/27	Deciphered Date	2019/12/27	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Power Train
					Size C
Date:		Thursday, June 06, 2019		Sheet	50 of 57

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2

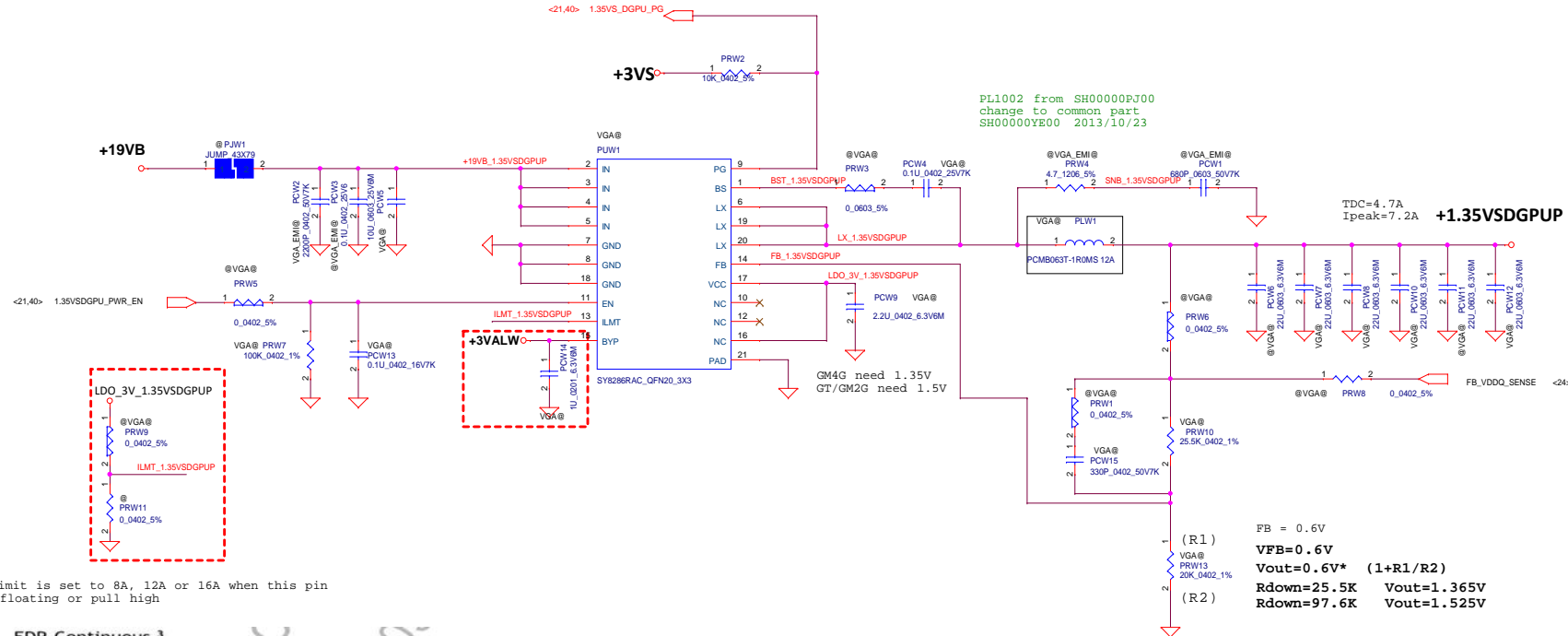


Table 6. EDP-Continuous<sup>3</sup>

Products	VRAM Type	GPU Core		GPU FBIO		FB Total <sup>1,5</sup>		1.05V Total <sup>2</sup>	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	2.0	—	4.2	0.80	0.06		
	DDR3/L	21.0	1.4	1.4	2.4	0.80	0.06		
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	0.80	0.06		
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	0.80	0.06		
N16S-GXR	DDR3/L	26.0	1.4	1.4	2.4	0.80	0.06		
	GDDR5	35.4	—	2.4	—	2.6	0.40		

Table 7. EDP-Peak<sup>3</sup>

Products	VRAM Type	GPU Core		GPU FBIO		FB Total <sup>1,5</sup>		1.05V Total <sup>2</sup>	
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1		
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1		
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1		
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1		
N16S-GXR	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1		
	GDDR5	54.0	—	4.6	—	9.5	2.9		

Table 7. Output EDP-Continuous

Product	NVVD	GPU FBIO	FB Total <sup>5</sup>	1.0V Total <sup>1</sup>	1.8V Total <sup>2</sup>
	(A)	(A)	(A)	(A)	(A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

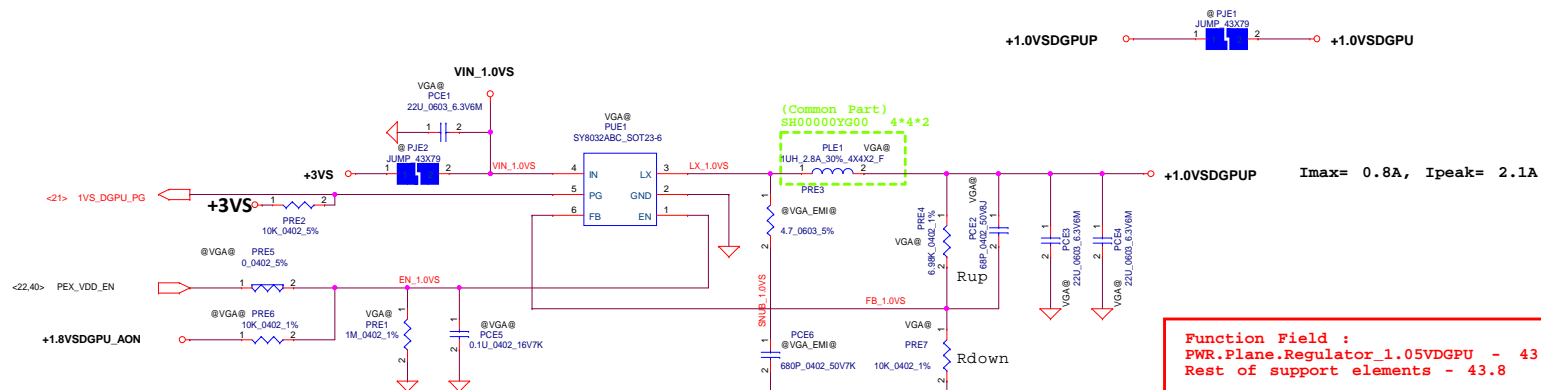
Table 8. Output EDP-Peak

Product	NVVD	GPU FBIO	FB TOTAL <sup>4</sup>	1.0V Total <sup>1</sup>
	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/12/27		Title	
Deciphered Date		2019/12/27		Power Train	
Document Number		EH7LW M/B LA-H791P		Rev	
Date		Thursday, June 06, 2019		Sheet	
51		of		57	



Module model information  
SY8032\_V2.mdd

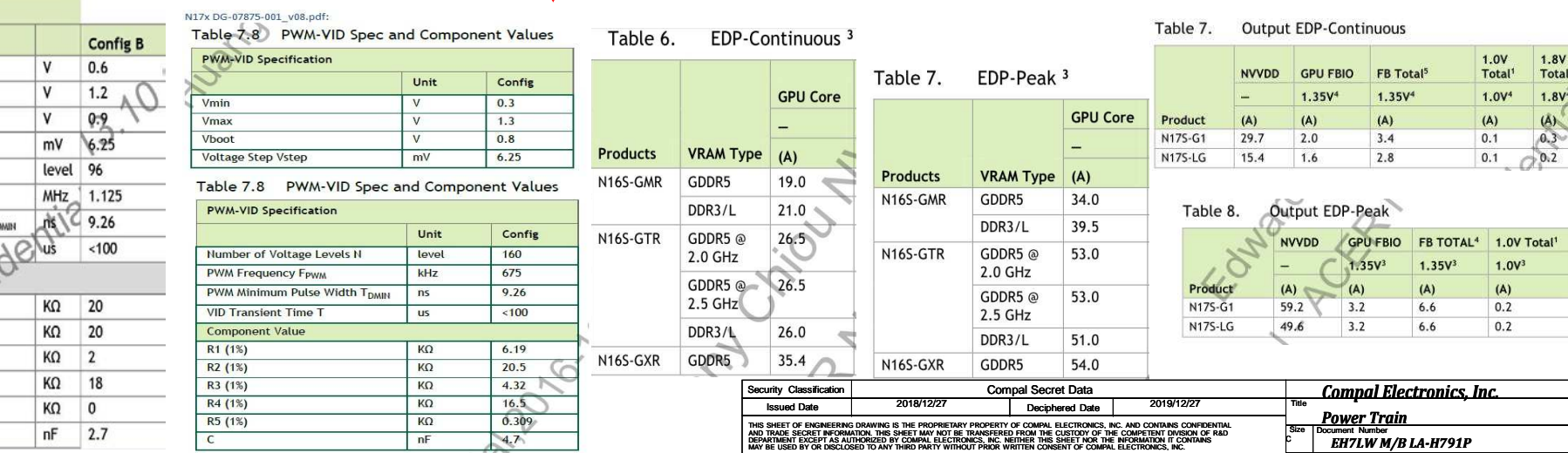


Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

$$\begin{aligned} V_{out} &= 0.6V * (1 + R_{up}/R_{down}) \\ N16 &= 1.05V \\ &= 0.6V * (1 + (7.68/10)) = 1.061 \quad (1.01\%) \\ &= 0.6V * (1 + (7.32/10)) = 1.039 \quad (-1\%) \\ N17 &= 1.0V \\ V_{out} &= 0.6V * (1 + (6.98/10)) = 1.019V \quad (1.02\%) \end{aligned}$$

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Power Train
				Size Document Number
				EH7LW M/B LA-H791P
				Rev 0.2
				Date: Thursday, June 06, 2019 Sheet 52 of 57

Figure 1: Schematic representation of the experimental design. The figure shows a 2x3 grid of conditions. The columns are labeled R1 and R2, and the rows are labeled R3 and R4. The conditions are: R1 (N16S\_VGA@ PR1209 20K\_0402\_1%), R2 (N16S\_VGA@ PR1208 20K\_0402\_1%), R3 (N16S\_VGA@ PR1211 2K\_0402\_1%), R4 (N16S\_VGA@ PR1210 18K\_0402\_1%), R5 (N16S\_VGA@ PR1224 0\_0402\_5%), and C (N16S\_VGA@ PC1210 2700P\_0402\_50V7K). Each condition is represented by a blue circle with a white dot in the center.



N17X DG-07875-001\_v08.pdf:

**Table 7.8 PWM-VID Spec and Component Values**

PWM-VID Specification		
	Unit	Config
V <sub>min</sub>	V	0.3
V <sub>max</sub>	V	1.3
V <sub>boot</sub>	V	0.8
Voltage Step V <sub>step</sub>	mV	6.25

**Table 7.8 PWM-VID Spec and Component Values**

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F <sub>PWM</sub>	kHz	675
PWM Minimum Pulse Width T <sub>DMIN</sub>	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Products		GPU Core
VRAM Type		(A)
N165-GMR	GDDR5	34.0
	DDR3/L	39.5
N165-GTR	GDDR5 @ 2.0 GHz	53.0
	GDDR5 @ 2.5 GHz	53.0
	DDR3/L	51.0
N165-GXR	GDDR5	54.0

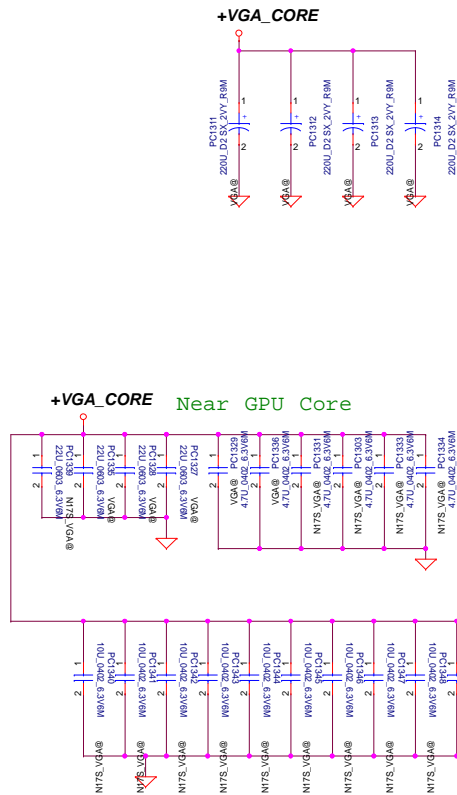
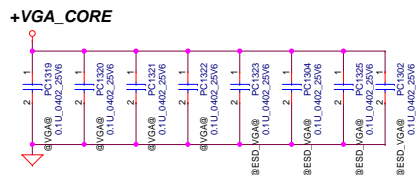
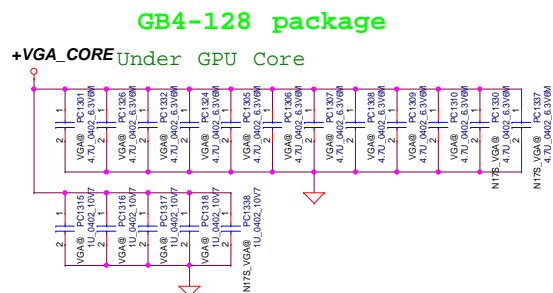
Table 7. Output EDP-Continuous					
	NVVDD	GPU FBIO	FB Total <sup>5</sup>	1.0V Total <sup>1</sup>	1.8V Total <sup>2</sup>
	—	1.35V <sup>4</sup>	1.35V <sup>4</sup>	1.0V <sup>4</sup>	1.8V <sup>4</sup>
Product	(A)	(A)	(A)	(A)	(A)
N175-G1	29.7	2.0	3.4	0.1	0.3
N175-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak				
	NVVDD	GPU FBIO	FB TOTAL <sup>4</sup>	1.0V Total <sup>1</sup>
	—	1.35V <sup>3</sup>	1.35V <sup>3</sup>	1.0V <sup>3</sup>
Product <sup>2</sup>	(A)	(A)	(A)	(A)
N175-G1	59.2	3.2	6.6	0.2
N175-LG	49.6	3.2	6.6	0.2

2019/12/27		<b>Compal Electronics, Inc.</b> <b>Power Train</b> Document Number <b>EH7LW M/B LA-H791P</b>	
CONTAINS CONFIDENTIAL STENT DIVISION OF RAD ATION, INC. CONTAINS ONICS, INC.		Size C	Rev



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>Power Train</b>	
Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					EH7LW M/B LA-H791P
				Date:	Thursday, June 06, 2019
				Sheet	54 of 57

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Reserve gpu prochot function	Reserve gpu prochot function		P.43	Del PQB8 for function reserve.	19.0103	EVT
02	change PL502 to common part	change PL502 to common part		P.44	change PL502 to common part(SH000016700)	19.0212	DVT
03	change PR1230 to 110K	change PR1230 to 110K for ocp setting		P.53	change PR1230 to 110K(SD034110380)	19.0212	DVT
04	change CAP size to 0402	change CAP size to 0402 for cost down		P.43,44	change PC302,PC502,PCB11 to SE00000W210 change PCB1 to SE074102K80	19.0212	DVT
05	change 0 ohm to R-short	change 0 ohm to R-short for cost down			change PR101,PR217,PR210,PRB15,PRB17,PRB23,PRB26,PRB16,PR304,PR505,PR502,PRM8,PRM11,PRM12,PRF3,PRF8,PRF1,PR1801,PRZ15,PRZ94,PRZ47,PRZ95,PRZ50,PRZ93,PRZ25,PRW5,PRW9,PRW6,PRW1,PRW3,PRE5,PR1231,PR1204,PR1218,PR1220,PR1201,PR1217,PR1213 to R-short (38PCS)	19.0212	DVT
06	DDR sequence	change PRM8 to 48.7K and PCM18 to 0.1u for sequence		P.38	change PRM8 to SD034487280 change PCM18 to SE102104K00	19.0215	DVT
07	CPU transient	change R and C value for CPU transient test		P.48	change PCZ11 to 330PuF(SE074331K80) change PRZ45 to 63.4k ohm(SD03463K280)(U42) change PRZ49 to 5.49k ohm(SD034549180)	19.0218	DVT
08	DDR sequence	change PRM8 to 0 ohm and del PCM18 for sequence		P.38	change PRM8 to SD028000080 del PCM18	19.0328	PVT
09	VR thermal alert adjust	change protect from 100c to 110c		P.48	change PHZ2,PHZ3 to SL200002I00, change PRZ51,PRZ66 to SD000000680, change PRZ52,PRZ69 to SD034332280, change PRZ67 to SD00000WS80,change PRZ63 to SD034130280, change PRZ70 to SD034137180,change PRZ68 to SD034392180, change PRZ64 to SD034976180,change PRZ71 to SD00000WS80,change PRZ74 to SD034165280	19.0507	pre MP
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							

WWW.ALISALER.COM

HW Schematic chang list (P.I.R)

Date	Rev.	Modify Item	Date	Rev.	Modify Item
1/25	0.2	Add cnvi cap(CM4) as intel request Swap JFP1 pin define update JI01 pin define update H12 hole,downdsize C2034/C2750			
1/29	0.2	update JI01 pin define change 0-ohm to R-short remove SWK1			
2/12	0.2	change RA3/RA4 to 0805 size			
3/13	1A	update UL2 pin28/pin29 pin define Add DA3/DA4 for audio ESD protection update JI01 footprint			
5/9	1B	update RC262 75k for CML			



HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
------	------	------	------	-------------------	-------------

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/12/27	Deciphered Date	2019/12/27	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		EH7LW M/B LA-H791P			Rev 0.2
		Date: Thursday, June 06, 2019			Sheet 57 of 57

WWW.ALISALER.COM